ANT-20, ANT-20E
Advanced Network Tester

Concatenated Mappings
OC-12c/STM-4c
OC-48c/STM-16c

BN 3035 /90.90 bis 3035/90.93

Software Version 7.20

Operating Manual

10

BN 3035/98.36

WAVETEK
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Communications Test Solutions

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Introduction

1 Concatenation options

1.1 OC-12c/STM-4c options

Modern bandwidth capacity requirements (e.g. Internet) have led to the setting up of networks with transmission capacities of up to 600 Mbit/s. These networks use concatenated containers from the SDH and SONET signal structures. The two methods of concatenation used are known as contiguous concatenation and virtual concatenation. One of the main applications for OC-12c or STM-4c signals is ATM. More and more OC-12c or STM-4c interfaces are being used in ATM exchange switches.

The “OC-12c/STM-4c” options for the ANT-20 allow you to test backbones, single connections or network elements. The options extend the main applications and instruments of the ANT-20 to cover these signal structures.

The following options are available:

- OC-12c/STM-4c ERROR TEST (BULK) (BN 3035/90.90)
- OC-12c/STM-4c ATM TESTING (BN 3035/90.91)
- OC-12v/STM-4v VIRTUAL CONCATENATION (BN 3035/90.92)

The “OC-12c/STM-4c ERROR TEST (BULK)” option can be used to test the performance of transmission paths. All of the ANT-20 analyzers can be used at the same time. Overhead Analyzer, Pointer Analyzer, Anomaly/Defect Analyzer, Jitter Analyzer and Performance Analysis allow correlation of the measurement results.

The “OC-12c/STM-4c ATM TESTING” option extends the applications of the ATM Module, BN 3035/90.70.

These two options are used to test the paths and network elements used for contiguous concatenation.

The “OC-12v/STM-4v VIRTUAL CONCATENATION” option extends the ANT-20 to cover this multiplexing and transmission method, which can be used by telecoms service providers to transmit concatenated VC-4 containers over existing SDH networks.

1.2 OC-48c/STM-16c options

Modern bandwidth capacity requirements (e.g. Internet) have led to the setting up of networks with transmission capacities of up to 2400 Mbit/s. These networks use concatenated containers from the SDH and SONET signal structures. One main application for OC-48c or STM-16c signals is for mapping STS-12c SPE or VC-4-4c containers that are filled with ATM signals. The use of OC-12c or STM-4c interfaces in ATM switches and the transmission of signals via OC-48 or STM-16 is becoming more common.

The “OC-48c/STM-16c” options for the ANT-20 allow you to test backbones, single connections or network elements. The options extend the main applications and instruments of the ANT-20 to cover these signal structures.

The following options are available:

- OC-12c/STM-4c ERROR TEST (BULK) (BN 3035/90.90)
- OC-12c/STM-4c ATM TESTING (BN 3035/90.91)
- OC-48c/STM-16v ERROR TEST (BULK) (BN 3035/90.93)

The “OC-12c/STM-4c ERROR TEST (BULK)” option and the “OC-48c/STM-16c ERROR TEST (BULK)” option can be used to test the performance of transmission paths. All of the ANT-20 analyzers can be used at the same time. Overhead Analyzer, Pointer Analyzer, Anomaly/Defect Analyzer, Jitter Analyzer and Performance Analysis allow correlation of the measurement results.

The “OC-12c/STM-4c ATM TESTING” option extends the applications of the ATM Module, BN 3035/90.70.

These three options are used to test the paths and network elements used for contiguous concatenation.

2 Applications

2.1 OC-12c/STM-4c

The “OC-12c/STM-4c” options expand the applications of the virtual instruments (VI) of the ANT-20 to include the following signal structures:

- STS-12c SPE Contiguous Concatenation
- STS-12v SPE Virtual Concatenation
- VC-4-4c Contiguous Concatenation
- VC-4-4v Virtual Concatenation

These signals have a payload bit rate of 599.040 Mbit/s.

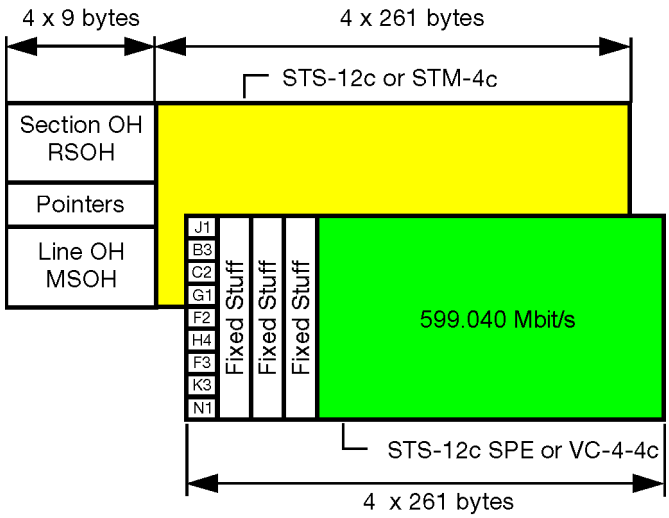


Fig. I-1 Contiguous concatenation, OC-12c/STM-4c

The “Signal Structure” VI can be used to set the appropriate mapping for concatenated containers for the transmitter (Tx) and receiver (Rx).

The following VIs can be used for tests after the settings are made:

- Performance Analyzer
- Anomaly/Defect Analyzer
- Anomaly/Defect Insertion
- Overhead Analyzer
- Overhead Generator
- Pointer Analyzer
- Pointer Generator
- Jitter Generator/Analyzer
- ATM Signal Structure
- ATM Traffic Analyzer
- ATM Background Load Generator

The “OC-12c/STM-4c ERROR TEST (BULK)” and “OC-12c/STM-4c ATM TESTING” options provide test functions for contiguous concatenation mapping.

With the “OC-12c/STM-4c ERROR TEST (BULK)” option, a bulk signal is mapped into the concatenated containers. With the “OC-12c/STM-4c ATM TESTING” option, cells are mapped into the containers.

The “OC-12v/STM-4v VIRTUAL CONCATENATION” option expands all test functions for bulk signal and cell mapping.

By combining the “OC-12c/STM-4c ATM TESTING” option with the ATM module and the “Jitter Generator/Analyzer 622 Mbit/s”, it is possible to demonstrate the conformance of ATM network elements to the jitter requirements of ITU-T, Bellcore and ANSI.

2.1.1 OC-12c/STM-4c TEST ERROR (BULK); (Contiguous Concatenation Mapping)

The “OC-12c/STM-4c ERROR TEST (BULK)” option is used to additionally analyze the bit error ratio for concatenated containers in accordance with ITU-T O.150. A selectable pseudo-random bit sequence is mapped into the concatenated container for this measurement.

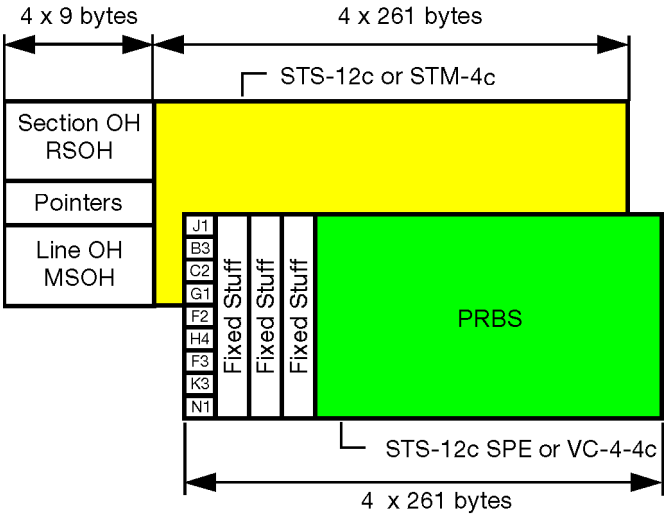


Fig. I-2 Contiguous concatenation, OC-12c/STM-4c TEST ERROR (BULK)

2.1.2 OC-12c/STM-4c ATM TESTING (Contiguous Concatenation Mapping)

The “OC-12c/STM-4c ATM TESTING” option expands the “ATM Module” option (BN 3035/90.70) for the ANT-20 to allow ATM tests at 622 Mbit/s.

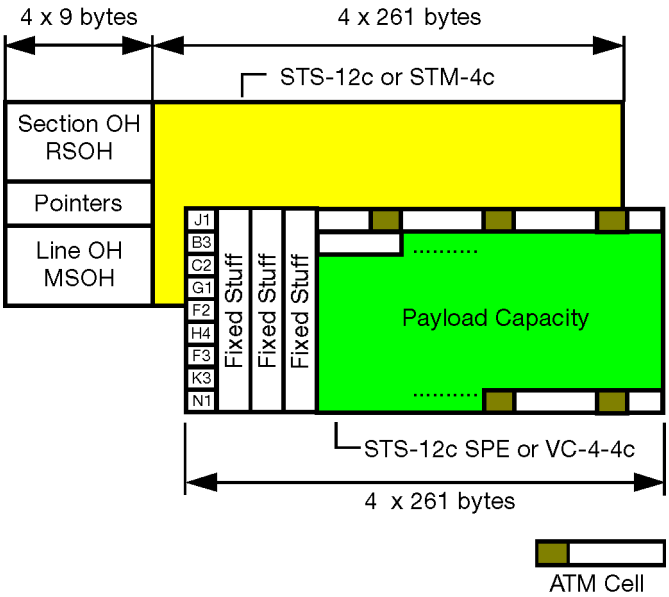


Fig. I-3 Contiguous concatenation, OC-12c/STM-4c ATM TESTING

2.1.3 OC-12v/STM-4v VIRTUAL CONCATENATION (Virtual Concatenation Mapping)

The “OC-12v/STM-4v VIRTUAL CONCATENATION” option provides additional test functions for this special mapping method.

OC-12vc/STM-4vc virtual concatenation signals have four AU-4-4 pointers instead of one AU-4-4 pointer.

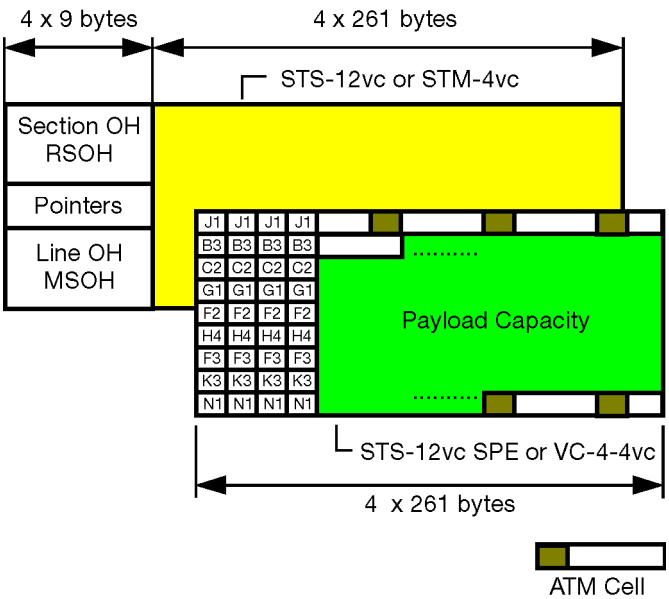


Fig. I-4 Virtual concatenation, OC-12v/STM-4v VIRTUAL CONCATENATION

This allows the VC-4-4v signal to be split into sub-VC-4 signals. The individual sub-VC-4 signals can be transmitted via different paths, resulting in different propagation delays for the containers. On termination in the receiver of the ANT-20, the individual VC-4s are recombined into a single signal.

The main application for the “OC-12v/STM-4v VIRTUAL CONCATENATION” option is in measuring the propagation delays of individual sub-VC-4s over the different transmission paths. The delay differences for the individual VC-4 containers can be measured if the Pointer Analyzer is also used. The delay differences for all four concatenated containers are displayed versus time, allowing you to assess the suitability of the selected paths for transmission.

Delta pointer actions can be directly set in the ANT-20 Pointer Generator to offset all four pointers of the concatenated container. In this way, termination in the interface modules of network elements can be tested. Such modules must be equipped with adequate buffers in order to equalize out possible differences in delay times.

The Overhead Generator and Overhead Analyzer can be used to manipulate, analyze and interpret the overhead bytes (SOH, POH or TOH).

2.2 OC-48c/STM-16c

The “OC-48c/STM-16c” options expand the applications of the virtual instruments (VI) of the ANT-20 to include the following signal structures:

- STS-48c SPE Contiguous Concatenation
- VC-4-16c Contiguous Concatenation
- STS-12c SPE Contiguous Concatenation
- VC-4-4c Contiguous Concatenation

These signals have a payload bit rate of 2396.160 Mbit/s or 599.040 Mbit/s.

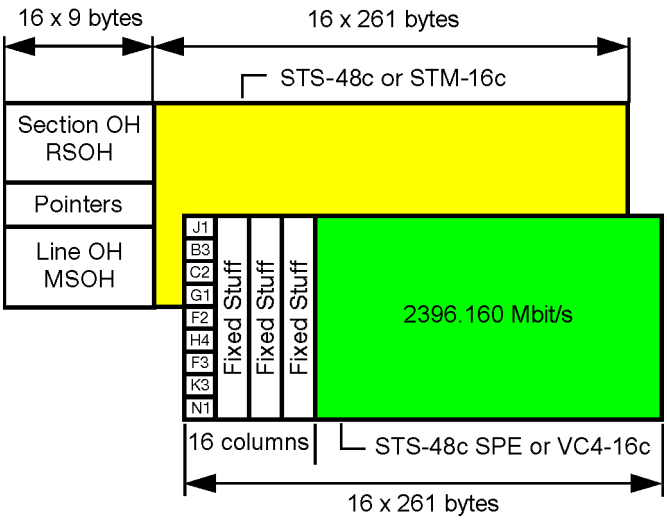


Fig. I-5 Contiguous concatenation, OC-48c/STM-16c

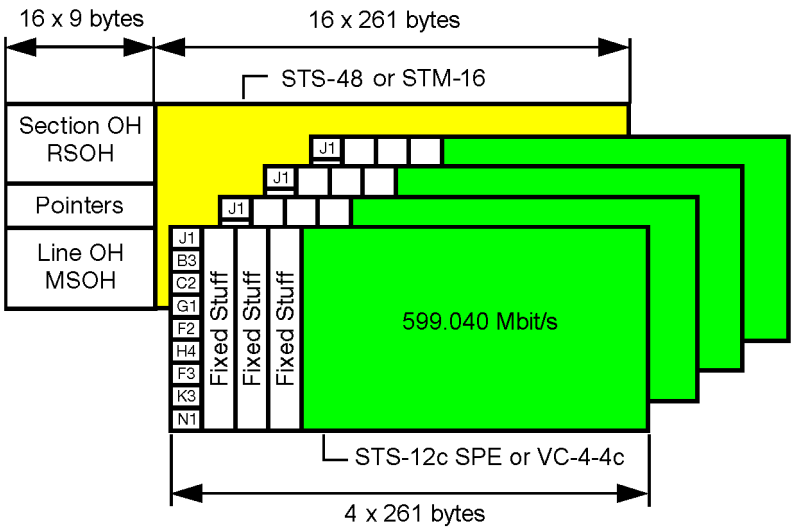


Fig. I-6 Contiguous concatenation, STS-12c SPE or VC-4-4c in OC-48c or STM-16c

The “Signal Structure” VI can be used to set the appropriate mapping for concatenated containers for the transmitter (Tx) and receiver (Rx).

The following VIs can be used for tests after the settings are made:

- Performance Analyzer
- Anomaly/Defect Analyzer
- Anomaly/Defect Insertion
- Overhead Analyzer
- Overhead Generator
- Pointer Analyzer
- Pointer Generator
- Jitter Generator/Analyzer
- ATM Signal Structure
- ATM Traffic Analyzer
- ATM Background Load Generator

The “OC-48c/STM-16c ERROR TEST (BULK)”, “OC-12c/STM-4c ERROR TEST (BULK)” and “OC-12c/STM-4c ATM TESTING” options provide test functions for contiguous concatenation mapping.

With the “OC-48c/STM-16c ERROR TEST (BULK)” and “OC-12c/STM-4c ERROR TEST (BULK)”options, a bulk signal is mapped into the concatenated containers. With the “OC-12c/ STM-4c ATM TESTING” option, cells are mapped into the containers.

By combining the “OC-12c/STM-4c ATM TESTING” option with the ATM module and the “Jitter Generator/Analyzer 622 Mbit/s”, it is possible to demonstrate the conformance of ATM network elements to the jitter requirements of ITU-T, Bellcore and ANSI.

2.2.1 OC-48c/STM-16c ERROR TEST (BULK); (Contiguous Concatenation Mapping)

The “OC-48c/STM-16c ERROR TEST (BULK)” option is used to additionally analyze the bit error ratio for concatenated containers in accordance with ITU-T O.150. A selectable pseudo-random bit sequence is mapped into the concatenated container for this measurement.

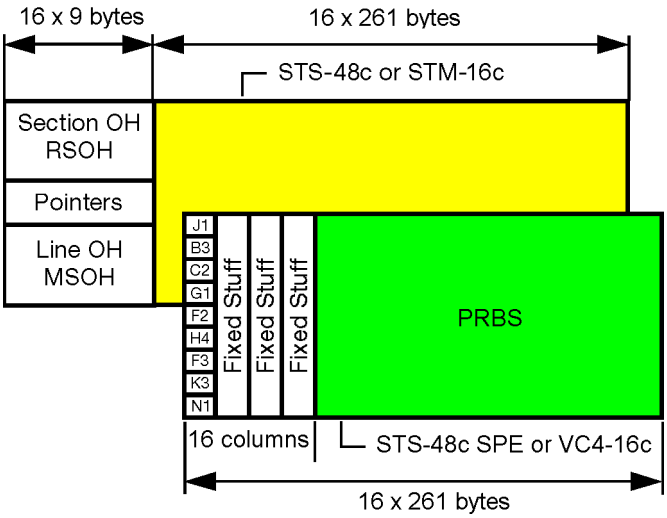


Fig. I-7 Contiguous concatenation, OC-48c/STM-16c ERROR TEST (BULK)

2.2.2 OC-12c/STM-4c ERROR TEST (BULK); (Contiguous Concatenation Mapping)

The “OC-12c/STM-4c ERROR TEST (BULK)” option is used to additionally analyze the bit error ratio for concatenated containers in accordance with ITU-T O.150. A selectable pseudo-random bit sequence is mapped into the concatenated container for this measurement.

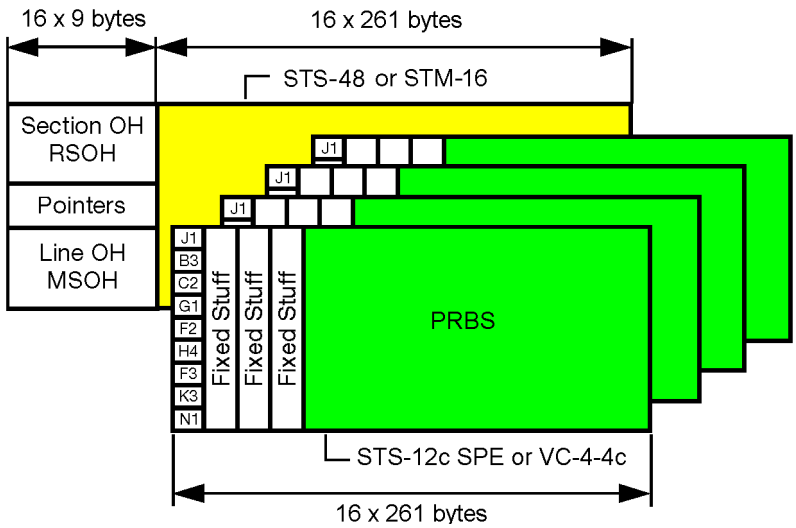


Fig. I-8 Contiguous concatenation, STS-12c SPE or VC-4-4c in OC-48c or STM-16c

2.2.3 OC-12c/STM-4c ATM TESTING (Contiguous Concatenation Mapping)

The “OC-12c/STM-4c ATM TESTING” option expands the “ATM Module” option (BN 3035/90.70) for the ANT-20 to allow ATM tests at 622 Mbit/s.

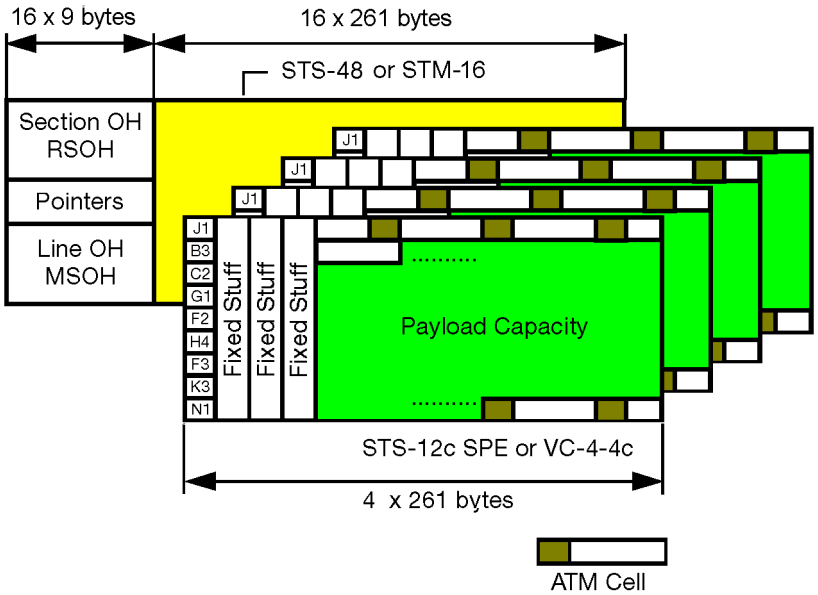


Fig. I-9 Contiguous concatenation and ATM tests, STS-12c/VC-4c in OC-48c or STM-16c

3 Operation

The “OC-12c/STM-4c” and “OC-48c/STM-16c” options do not alter the basic operating procedures for the virtual instruments. Signal structures for these options are set in the “Signal Structure” VI by means of the “CONCAT.” button.

Other additions are found in the Operating Manual for the Mainframe Instrument under the descriptions of the various virtual instruments in file section 4:

- Pointer Analyzer
- Pointer Generator
- Overhead Analyzer
- Overhead Generator
- Signal Structure

For ATM applications, additions are found in file section 8 of the ANT-20 Options File.

Specifications OC-12c/STM-4c

These specifications apply to the following options:

OC-12c/STM-4c mapping

OC-12c/STM-4c ERROR TEST (BULK). . . . . .BN 3035/90.90
OC-12c/STM-4c ATM TESTING. . . . . .BN 3035/90.91
OC-12v/STM-4v VIRTUAL CONCATENATION . . . . . .BN 3035/90.92

The numbers in square brackets […] against the measurement connections correspond to the numbers printed on the instrument.

Calibrated specifications are marked ***.

1 Generator section

1.1 Digital signal output

1.1.1 Signal output [18], optical

Connector . . . . . 2.5 mm (PC)

"Fiber to fiber" test adapter for connecting various
2.5 mm plug connectors . . . . . see list of accessories

Output level *** . . . . . 0 dBm +2/-3 dBm

Reduction in output level
for dual wavelength version . . . . . < 0.5 dBm

Output signal pulse shape . . . . . .to ITU-T G.957

Wavelength (switchable, depending on option) . . . . . .1310 nm (1280 to 1330 nm),
1550 nm (1480 to 1580 nm)

Laser safety class as per EN 60825-1:1994 1

The generator meets the requirements of ITU-T G.957 classes L1.1, L1.2, L1.3, L4.1, L4.2, L4.3.
Classes S1.1, S1.2 as well as S4.1 and S4.2 can be achieved by inserting an optical attenuator or the Optical Power Splitter BN 3035/90.49.

LASER ON status display

LED is on when the laser source is active.

1.2 Clock generation and bit rates

1.2.1 Clock generation

See “Specifications” for the mainframe instrument.

1.2.2 Bit rate

OC-12c/STM-4c. . . . . 622.08 Mbit/s

1.3 SDH and SONET Tx signals

- OC-12c signal generated as per Bellcore GR-253 Standard.
- STM-4c signal generated as per ITU-T Recommendation G.707.

1.3.1 OC-12c/STM-4c Tx signal

OC-12c/STM-4c signal formation:

- Signal generated internally, payload contains bulk signal or ATM cells.
- Complete signal taken from receiver.

1.3.2 Scrambling

Scrambling is as per ITU-T Recommendation G.707.
Scrambling can be activated or deactivated.

1.3.3 Overhead generation

1.3.3.1 Section overhead (SOH), Transport overhead (TOH)

Standard OC-12c/STM-4c overhead (hex)

	S O H, TOH																																							
1	A1 F6	A1 F6	A1 F6	A1 F6	A1 F6	A1 F6	A1 F6	A1 F6	A1 F6	A1 F6	A1 F6	A1 F6	A1 F6	A2 28	A2 28	A2 28	A2 28	A2 28	A2 28	A2 28	A2 28	A2 28	A2 28	A2 28	A2 28	J0 C1 01	Z0 C1 AA	Z0 C1 AA	Z0 C1 AA	— AA	— AA	— AA	— AA	— AA	— AA	— AA	— AA	— AA	— AA	— AA
2	B1 XX	— 00	— 00	— 00	— 00	— 00	— 00	— 00	— 00	— 00	— 00	— 00	— 00	E1 00	— 00	— 00	— 00	— 00	— 00	— 00	— 00	— 00	— 00	— 00	— 00	F1 00	— 00	— 00	— 00	— 00	— 00	— 00	— 00	— 00	— 00	— 00	— 00	— 00	— 00	— 00
3	D1 00	— 00	— 00	— 00	— 00	— 00	— 00	— 00	— 00	— 00	— 00	— 00	— 00	D2 00	— 00	— 00	— 00	— 00	— 00	— 00	— 00	— 00	— 00	— 00	— 00	D3 00	— 00	— 00	— 00	— 00	— 00	— 00	— 00	— 00	— 00	— 00	— 00	— 00	— 00	— 00
4a	H1 68	Y 9B	Y 9B	Y 9B	Y 9B	Y 9B	Y 9B	Y 9B	Y 9B	Y 9B	Y 9B	Y 9B	Y 9B	H2 00	— FF	— FF	— FF	— FF	— FF	— FF	— FF	— FF	— FF	— FF	— FF	H3 00	H3 00	H3 00	H3 00	H3 00	H3 00	H3 00	H3 00	H3 00	H3 00	H3 00	H3 00	H3 00	H3 00	H3 00
4b	H1 68	H1 68	H1 68	H1 68	Y 9B	Y 9B	Y 9B	Y 9B	Y 9B	Y 9B	Y 9B	Y 9B	Y 9B	H2 00	H2 00	H2 00	H2 00	— FF	— FF	— FF	— FF	— FF	— FF	— FF	— FF	H3 00	H3 00	H3 00	H3 00	H3 00	H3 00	H3 00	H3 00	H3 00	H3 00	H3 00	H3 00	H3 00	H3 00	H3 00
4c	H1 60	Y 93	Y 93	Y 93	Y 93	Y 93	Y 93	Y 93	Y 93	Y 93	Y 93	Y 93	Y 93	H2 00	— FF	— FF	— FF	— FF	— FF	— FF	— FF	— FF	— FF	— FF	— FF	H3 00	H3 00	H3 00	H3 00	H3 00	H3 00	H3 00	H3 00	H3 00	H3 00	H3 00	H3 00	H3 00	H3 00	H3 00
4d	H1 60	H1 60	H1 60	H1 60	Y 93	Y 93	Y 93	Y 93	Y 93	Y 93	Y 93	Y 93	Y 93	H2 00	H2 00	H2 00	H2 00	— FF	— FF	— FF	— FF	— FF	— FF	— FF	— FF	H3 00	H3 00	H3 00	H3 00	H3 00	H3 00	H3 00	H3 00	H3 00	H3 00	H3 00	H3 00	H3 00	H3 00	H3 00
5	B2 XX	B2 XX	B2 XX	B2 XX	B2 XX	B2 XX	B2 XX	B2 XX	B2 XX	B2 XX	B2 XX	B2 XX	B2 XX	K1 00	— 00	— 00	— 00	— 00	— 00	— 00	— 00	— 00	— 00	— 00	— 00	K2 00	— 00	— 00	— 00	— 00	— 00	— 00	— 00	— 00	— 00	— 00	— 00	— 00	— 00	— 00
6	D4 00	— 00	— 00	— 00	— 00	— 00	— 00	— 00	— 00	— 00	— 00	— 00	— 00	D5 00	— 00	— 00	— 00	— 00	— 00	— 00	— 00	— 00	— 00	— 00	— 00	D6 00	— 00	— 00	— 00	— 00	— 00	— 00	— 00	— 00	— 00	— 00	— 00	— 00	— 00	— 00
7	D7 00	— 00	— 00	— 00	— 00	— 00	— 00	— 00	— 00	— 00	— 00	— 00	— 00	D8 00	— 00	— 00	— 00	— 00	— 00	— 00	— 00	— 00	— 00	— 00	— 00	D9 00	— 00	— 00	— 00	— 00	— 00	— 00	— 00	— 00	— 00	— 00	— 00	— 00	— 00	— 00
8	D1 0 00	— 00	— 00	— 00	— 00	— 00	— 00	— 00	— 00	— 00	— 00	— 00	— 00	D1 1 00	— 00	— 00	— 00	— 00	— 00	— 00	— 00	— 00	— 00	— 00	— 00	D1 2 00	— 00	— 00	— 00	— 00	— 00	— 00	— 00	— 00	— 00	— 00	— 00	— 00	— 00	— 00	— 00
9	S1 00	Z1 00	Z1 00	Z1 00	Z1 00	Z1 00	Z1 00	Z1 00	Z1 00	Z1 00	Z1 00	Z1 00	Z1 00	Z2 00	Z2 00	M1 00	Z2 00	Z2 00	Z2 00	Z2 00	Z2 00	Z2 00	Z2 00	Z2 00	Z2 00	E2 00	— 00	— 00	— 00	— 00	— 00	— 00	— 00	— 00	— 00	— 00	— 00	— 00	— 00	— 00	— 00

Table S-1 SOH, TOH contents; OC-12c/STM-4c

XX: Inserted through parity formation (B1, B2)

Line 4a: SDH pointers (VC-4-4c)

Line 4b: SDH pointers (VC-4-4v)

Line 4c: SONET pointers (STS-12c)

Line 4d: SONET pointers (STS-12v)

H1 and H2 depend on the pointer address setting (pointer address = 0 is shown). H3 depends on whether a pointer action takes place.

Contents of SOH bytes

- Static bytes: All except B1, B2, H1, H2, H3
- Overhead sequence m, n, p: All except B1, B2, H1, H2, H3
- Trace Identifier: J0 (length = 16 frames with CRC7 formation)
- Dynamic bytes filled with PRBS11: E1, F1, E2 (single byte)
- Dynamic bytes filled with PRBS11: D1 to D3, D4 to D12 (byte group)
- Dynamic bytes via DCC/ECC interface, socket [21] (V.11): E1, F1, E2 (single byte)
- Dynamic bytes via DCC/ECC interface, socket [21] (V.11): D1 to D3, D4 to D12, K1 to K2 (byte group)

1.3.4 VC-4c path overhead (POH), high-order

1.3.4.1 Contiguous concatenation (VC-4-4c)

Standard overhead

POH byte	**POH #1**	**POH #2 to #4** Fixed stuffing (3 columns)
J1 (ASCII)	“WG HP-TRACE”	“00”
B3 (hex)	Inserted by parity formation	“00”
C2 (hex)	“13” for ATM mapping “FE” for BULK (STM-4) “01” for BULK (OC-12)	“00”
G1 (hex)	“00”	“00”
F2 (hex)	“00”	“00”
H4 (hex)	“FF”	“00”
F3 (hex)	“00”	“00”
K3 (hex)	“00”	“00”
N1 (hex)	“00”	“00”

Table S-2 POH contents

Contents of VC-4-4c POH bytes

- Static bytes: All except B3, H4
- Overhead sequence m, n, p: All except B3, H4
- Trace Identifier: J1 (length = 16 frames with CRC7 formation)
- Dynamic bytes filled with PRBS11: F2 (byte)
- Dynamic bytes via DCC/ECC interface (V.11): F2, K3, N1 (byte)
- H4 sequence, switchable, 4 / 48 bytes

1.3.4.2 Virtual concatenation (VC-4-4v)

Only with option BN 3035/90.92

Standard overhead

POH byte	POH #1	POH #2 to #4
J1 (ASCII)	“WG HP-TRACE”	“00”
B3 (hex)	Inserted through parity formation	
C2 (hex)	“13” for ATM mapping “FE” for BULK signal (STM-4) “01” for BULK (OC-12)	“13” for ATM mapping “FE” for BULK signal (STM-4) “01” for BULK (OC-12)
G1 (hex)	“00”	“00”
F2 (hex)	“00”	“00”
H4 (hex)	“FF”	
F3 (hex)	“00”	“00”
K3 (hex)	“00”	“00”
N1 (hex)	“00”	“00”

Table S-3 POH contents

Contents of VC-4-4v POH byte #1

- Static bytes: All except B3, H4
- Overhead sequence m, n, p: All except B3, H4
- Trace Identifier: J1 (length = 16 frames with CRC7 formation)
- Dynamic bytes with PRBS11: F2 (byte)
- Dynamic bytes via DCC/ECC interface (V.11): F2, K3, N1 (byte)
- H4 sequence, switchable, 4 / 48 bytes

Contents of VC-4-4v POH bytes #2 to #4

- Static bytes: All except B3, H4
- All bytes as POH #1, except B3

1.3.5 Generation of pointer actions

1.3.5.1 Contiguous concatenation

Stimulation

AU-4 pointer sequences

See “STM-1 mapping” and “STS-1 mapping” specifications.

Pointer jumps

Pointer jump from pointer value A to pointer value B (including setting a new pointer).

Pointer jumps are executed using NDF.
Pointer range A + B:

AU-4 . . . . . 0 to 782

1.3.5.2 Virtual concatenation

Only with option BN 3035/90.92

Stimulation of pointer #1

AU-4 pointer sequences

See “STM-1 mapping” and “STS-1 mapping” specifications.

Pointer jumps

Pointer jump from pointer value A to pointer value B (including setting a new pointer).

Pointer jumps are executed using NDF.
Pointer range A + B:

AU-4 . . . . . 0 to 782

Stimulation of pointers #2 to #4

Pointer actions in pointer #1 affect pointers #2 to #4 at the same time.

A delta value (deviation) from pointer #1 can be generated for pointers #2 to #4.

Maximum delta of pointers #2 to #4 to pointer #1 . . . . . ± 40 pointers
or time . . . . . ± 6.17 µs

Increment / decrement. . . . . 1 pointer
or time . . . . . 154 ns

Setting a new delta value is through n x increment or n x decrement.

For n > 1, the spacing between two consecutive increment / decrement actions is 32 frames (4 ms).

The delta for pointers #2 to #4 is retained for pointer actions in pointer #1.

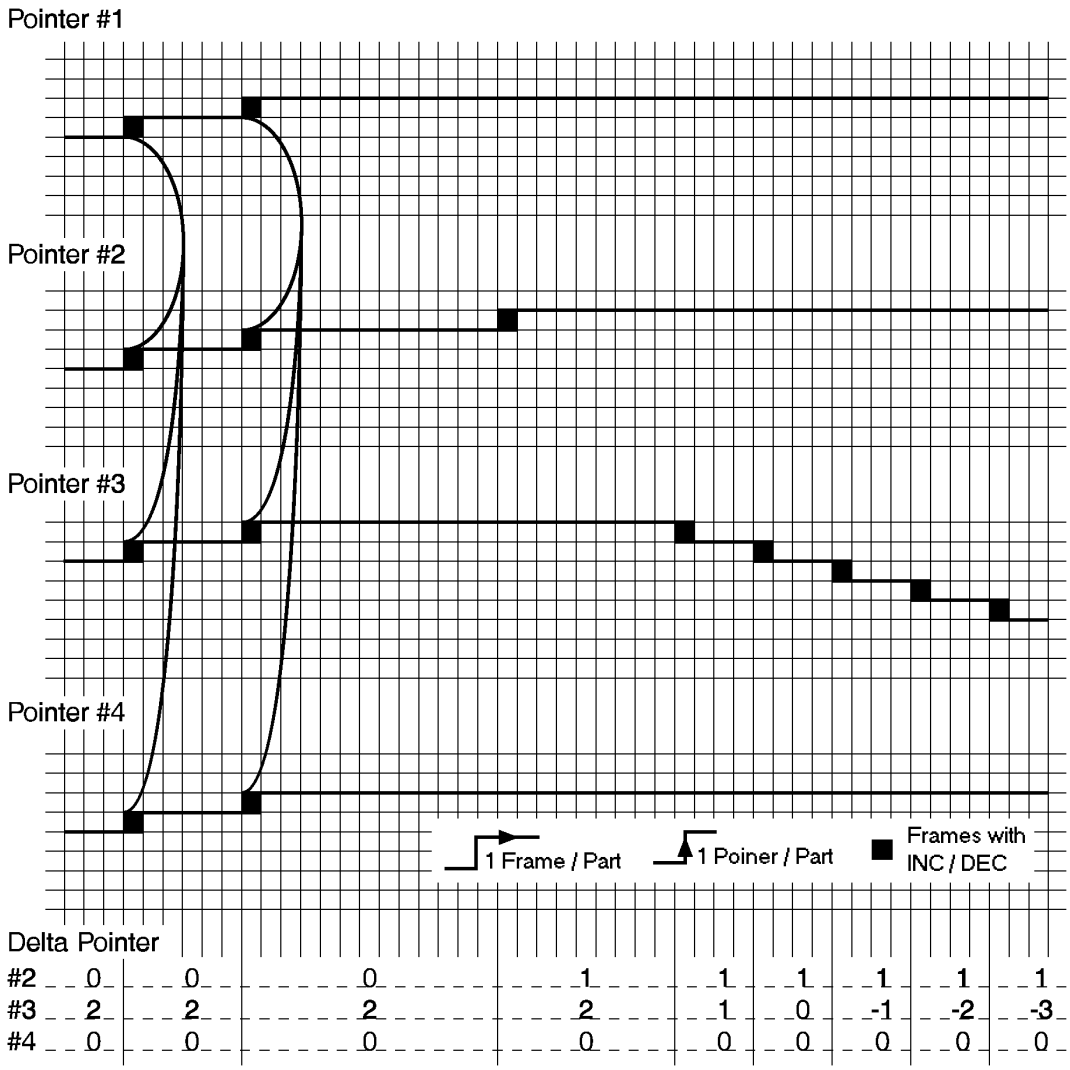


Fig. S-1 Pointer actions

1.3.6 OC-12c/STM-4c anomaly insertion

Anomaly insertion . . . . . B1, B2, B3 parity errors
REI-L/MS-REI, REI-P/HP-REI

Trigger modes . . . . . .Single
or Rate

A bit error rate is inserted when Rate is selected.

Anomaly	**Single**	**Rate**[1]
B1 (OC-12c, STM-4c)	yes	2E-4 to 1E-10
B2 (OC-12c, STM-4c)	yes	2E-3 to 1E-10
REI-L (OC-12c) MS-REI (STM-4c)	yes	2E-3 to 1E-10
B3[2] (STS-12c SPE/VC-4-4c)	yes	2E-4 to 1E-10
REI-P (STS-12c SPE)[3] HP-REI (VC-4-4c)	yes	2E-4 to 1E-10

1 Mantissa: 1 to 9, Exponent: -1 to -10 (integer values)
2 Virtual concatenation: Single: POH #1; Rate: All four POHs
3 Virtual concatenation: Insertion in POH #1

Table S-4 Anomalies (OC-12c, STM-4c) and trigger modes

Insertion of **anomalies** and **defects** is mutually exclusive. The action first selected is active; the second action is rejected.

1.3.7 OC-12c/STM-4c defect generation

Defect	Sensor function test	Sensor threshold test	
-	On/Off	M in N	|---t1---| |------t2------|
LOS (optical)	yes	M = 800 to 7200 N = 1600 to 8000	t1 = 0.1 to 60.0 s t2 = 0.2 to 600 s
LOF-622	yes	M = 1 to N - 1 N = 1 to 8000	t1 = 0.1 to 60.0 s t2 = 0.2 to 600 s
TIM-L (OC-12c) RS-TIM (STM-4c)	yes	-	-
AIS-L (OC-12c) MS-AIS (STM-4c)	yes	M = 1 to N - 1 N = 1 to 8000	t1 = 0.1 to 60.0 s t2 = 0.2 to 600 s
RDI-L (OC-12c) MS-RDI (STM-4c)	yes	M = 1 to N - 1 N = 1 to 8000	t1 = 0.1 to 60.0 s t2 = 0.2 to 600 s
LOP_P (STS-12c SPE) AU-LOP (VC-4-4c)[1]	yes	M = 1 to N - 1 N = 1 to 8000	t1 = 0.1 to 60.0 s t2 = 0.2 to 600 s
LOP-Cx[2]	yes	M = 1 to N - 1 N = 1 to 8000	t1 = 0.1 to 60.0 s t2 = 0.2 to 600 s
AIS-P (STS-12c SPE) AU-AIS (VC-4-4c)[1]	yes	M = 1 to N - 1 N = 1 to 8000	t1 = 0.1 to 60.0 s t2 = 0.2 to 600 s
AIS-Cx[2]	yes	M = 1 to N - 1 N = 1 to 8000	t1 = 0.1 to 60.0 s t2 = 0.2 to 600 s
UNEQ-P (STS-12c SPE) HP-UNEQ (VC-4-4c)	yes	M = 1 to N - 1 N = 1 to 8000	t1 = 0.1 to 60.0 s t2 = 0.2 to 600 s
PLM-P (STS-12c SPE) HP-PLM (VC-4-4c)	yes	M = 1 to N - 1 N = 1 to 8000	t1 = 0.1 to 60.0 s t2 = 0.2 to 600 s
RDI-P (STS-12c SPE) HP-RDI (VC-4-4c)	yes	M = 1 to N - 1 N = 1 to 8000	t1 = 0.1 to 60.0 s t2 = 0.2 to 600 s
TIM-P (STS-12c SPE) HP-TIM (VC-4-4c)	yes	-	-

1 Insertion in all four pointers (AU-4)
2 X = 1 to 4; insertion in selected pointer (AU-4) only

Table S-5 Defects

Insertion of **defects** and **anomalies** is mutually exclusive. The action first selected is active; the second action is rejected.

1.4 Payload generation

1.4.1 BULK signal generator

Only with option BN 3035/90.90

1.4.1.1 Payload

Bit rate . . . . . 599.04 Mbit/s

Structure . . . . . unframed

1.4.1.2 Bit patterns

Digital word . . . . . .16 bits

Pseudo-random bit sequences . . . . . PRBS 15, PRBS 15 inverted, PRBS 20, PRBS 23, PRBS 23 inverted, PRBS 31, PRBS 31 inverted

1.4.1.3 Anomaly insertion

The following anomaly can be inserted in addition to those described in Sec. 1.3.6, Page S-7:

Anomaly	**Single**	**Rate[1]**
TSE	yes	1E-2 to 1E-9
1 Mantissa: 1, Exponent -2 to -9 (integer values)		

Table S-6 Additional anomaly (OC-12c, STM-4c)

Anomaly insertion . . . . . .Test sequence error (TSE)

Trigger modes . . . . . Single or Rate

Insertion of **anomalies** and **defects** is mutually exclusive. The action first selected is active; the second action is rejected.

1.4.2 ATM generator section

Only with options BN 3035/90.70 (ATM Module) and BN 3035/90.91

1.4.2.1 Scrambling

Scrambling is according to ITU-T Recommendation I.432 ($X^{43}+1$). The function can be disabled.

1.4.2.2 Anomaly insertion

The following anomalies can be inserted in addition to those described in Sec. 1.3.6, Page S-7.

Anomaly	**Single**	**Rate[1]**	**Sensor threshold**
			M in N
HEC uncor.[2]	yes	1E-2 to 1E-6	M = 1 to 31 N = M + 1 to M + 31
HEC cor.[3]	yes	1E-2 to 1E-6	M = 1 to 31 N = M + 1 to M + 31
AAL-1 cell loss	yes	1E-3 to 1E-6	-
AAL-1 CRC	yes	1E-3 to 1E-6	-
AAL-1 PE	yes	1E-3 to 1E-6	-

1 Mantissa: 1 only, Exponent: -1 to -6 (integer values)
2 Uncorrectable header error
3 Correctable header error

Table S-7 Additional anomalies

The AAL-1 cell loss, AAL-1 CRC and AAL-1 PE anomalies refer to the measurement channel. Test sequence errors (TSE) are inserted in the ATM payload or in the AAL-1 payload of the test channel.

Correctable and uncorrectable header errors are inserted in the overall cell stream.

1.4.2.3 Defect generation

The following defects can be generated in addition to those described in Sec. 1.3.7, Page S-9.

Defect	Sensor function test	Single
	On / Off	
LCD[1]	yes	yes
VP-AIS	yes	yes
VP-RDI	yes	yes
VC-AIS[2]	yes	yes
VC-RDI[3]	yes	yes
Vx-AIS[4]	yes	yes
Vx-RDI[4]	yes	yes

1 LCD (Loss of Cell Delineation) is generated by uncorrectable header errors in ≥ 7 consecutive cells.
2 AIS: Alarm Indication Signal; VC: Virtual Channel; VP: Virtual Path
3 RDI: Remote Defect Indication
4 For Vx-AIS and Vx-RDI defects are inserted in the VP and VC in parallel.

Table S-8 Additional defects

1.4.2.4 Test channel

Cells

Header

UNI/NNI, VCI, VPI, PT and CLP . . . . . settable
HEC . . . . . formed automatically

Payload

Pseudo-random bit sequences . . . . . PRBS 11, PRBS 15, PRBS 20, PRBS 23
Digital word . . . . . 16 bits

Load profiles

Constant, Equidistant, Burst

Constant load profile

Load setting . . . . . 14.976 to 149760 kbit/s

Resolution dependent on load range setting
14.976 to 1482.624 kbit/s . . . . . 14.976 kbit/s
149.76 to 14826.24 kbit/s . . . . . 149.76 kbit/s
1497.6 to 149760 kbit/s. . . . . 1497.6 kbit/s

Equidistant load profile setting range

Cell spacing . . . . . 4 to 40000 cell periods
Maximum cell spacing deviation. . . . . ± 1 cell period

Resolution depending on cell spacing range setting
4 to 400 . . . . . 4 cell periods
40 to 4000 . . . . . 40 cell periods
400 to 40000 . . . . . 400 cell periods

Burst load profile setting range

Maximum burst length . . . . . 4092 cells / 2.79 ms
Burst load . . . . . 1497.6 to 149760 kbit/s
Resolution . . . . . depends on burst length

Maximum burst period . . . . . 131068 cells / 89 ms

Load units . . . . . Mbit/s, Cells/s, %
Time units . . . . . cell period

1.4.2.5 Background load

A channel is generated as background load. The test channel has priority.

Header . . . . . freely selectable

Payload . . . . . byte by byte constant, bytes freely selectable

Load profile . . . . . CBR, Fill

Constant bit rate (CBR) . . . . . 449280 kbit/s

Filling up to . . . . . 149760 / 599040 kbit/s

1.4.2.6 Fill cells

The cell stream is filled with IDLE or UNASSIGNED cells. Either can be selected.

1.4.2.7 AAL-1 segmentation

PDU signals with system bandwidths of 1,5 Mbit/s, 2 Mbit/s, etc. can be transmitted in the AAL-1 in the test channel.

Possible payload patterns for 2 Mbit/s . . . . . PRBS unframed,
PRBS in PCM30,
PRBS in PCM30CRC

2 Receiver section

2.1 Digital signal inputs

2.1.1 Signal input [17], optical

Connector . . . . . 2.5 mm (PC)

Fiber to fiber" test adapter for connecting various
2.5 mm plug connectors . . . . . see list of accessories

Input sensitivity
OC-12c / STM-4c *** . . . . . -8 to -28 dBm

Max. permissible input level . . . . . +2 dBm

Wavelength . . . . . 1100 to 1580 nm

The receiver meets the requirements of ITU-T G.957 Classes S1.1, S1.2, S4.1, S4.2 and S4.3.

Tolerance to jitter

measured using scrambled SDH or SONET signals:

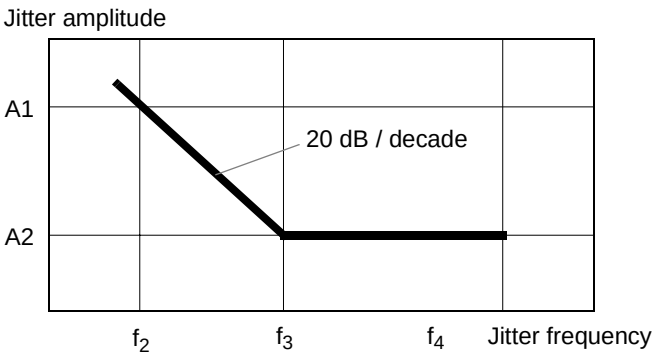


Fig. S-2 Jitter amplitude versus jitter frequency

Bit rate Mbit/s	**A1 Ulpp**	**f_2 kHz**	**A2 Ulpp**	**f_3 kHz**	**f_4 kHz**
51.840	1.5	2	0.15	20	500
155.520	1.5	6.5	0.15	65	1300
622.080	1.5	25	0.15	250	5000

Table S-9 ANT-20 tolerance to jitter at system bit rates

2.1.2 Signal input [16], electrical

Connector . . . . . unbalanced (coaxial)

Socket type . . . . . SMA

Input impedance . . . . . 50 Ω

Line code . . . . . NRZ (scrambled)

Input voltage range . . . . . 200 mVpp to 1Vpp

Bit rate . . . . . 155.52 Mbit/s; 622.08 Mbit/s

Tolerance to jitter

See Tab. S-9, Page S-14

LOS (Loss of Signal) status display

The LED is on if the signal input is active but no signal is present.

2.1.3 Clock recovery

See “Specifications” for the mainframe instrument.

2.2 SDH and SONET Rx signals

- Evaluation of an OC-12c signal as per Bellcore GR-253 standard.
- Evaluation of a STM-4c signal as per ITU-T Recommendation G.707.

2.2.1 OC-12c/STM-4c Rx signal

Evaluation of OC-12c/STM-4c signals:

- Analysis of the transport overhead (TOH) / section overhead (SOH), path overhead (POH) and payload (BULK), either directly or in conjunction with the ATM Module (option BN 3035/90.70).
- Analysis of the transport overhead (TOH) / section overhead (SOH) and loop through of the OC-12c/STM-4c signal to the generator (D&C)

2.2.2 Descrambling

Descrambling is according to ITU-T Recommendation G.707.
Descrambling can be activated / deactivated.

Tip: Make sure that there are no long sequences of zeros or ones in the data stream of unscrambled input signals.

2.3 Measurement modes

2.3.1 Evaluation of section overhead (SOH), transport overhead (TOH)

Display

Complete SOH, TOH: (four channel-associated part SOH) . . . . . hexadecimal

Trace Identifier J0 (STS-12c SPE/VC-4-4c) . . . . . ASCII, plain text

Overhead Capture . . . . . see Section 1 "Extended Overhead Analysis" option BN 3035/90.15

Evaluation

Bit error rate test

using pseudo-random bit sequence PRBS11 . . . . . E1, F1, E2 (single byte)

using pseudo-random bit sequence PRBS11 . . . . . .D1 to D3, D4 to D12 (byte group)

Output

The overhead channels are output via the

DCC/ECC interface, socket [21] (V.11) . . . . . E1, F1, E2 (single byte)

DCC/ECC interface, socket [21] (V.11) . . . . . D1 to D3, D4 to D12, K1 to K2 (byte group)

2.3.2 Evaluation of path overhead (POH)

2.3.2.1 Contiguous concatenation

Display

Complete POH . . . . . hexadecimal

Trace Identifier J1 . . . . . ASCII, plain text

Evaluation

Bit error rate test

using pseudo-random bit sequence PRBS11 . . . . . F2

Output

The overhead channels are output via the

DCC/ECC interface, socket [21] (V.11) F2, N1

2.3.2.2 Virtual concatenation

Display

Complete POH: (four channel-associated part POH) . . . . . hexadecimal

Trace Identifier J1 (POH #1 only) . . . . . .ASCII, plain text

Evaluation

Bit error rate test

using pseudo-random bit sequence PRBS11 (POH #1 only) F2

Output

The overhead channels are output via the

DCC/ECC interface, socket [21] (V.11) (POH #1 only) F2, N1

2.3.3 Measurement of AU pointer actions

Evaluation

The AU pointer (pointer #1 in virtual concatenation) is indicated as an absolute value. The direction and number of pointer movements are detected.

NDF (new data flag) is detected and counted (pointer #1 in virtual concatenation).

The differences (delta) between the pointer values of pointers #2 to #4 and pointer #1 are determined and recorded (virtual concatenation).

Maximum delta . . . . . ± 40 pointers / ± 6.17 µs

Display

- Number of AU pointer operations (pointer #1 in virtual concatenation):
  Increments, decrements, sum of increments + decrements,
  difference of increments - decrements
- Pointer address (pointer #1 in virtual concatenation)
- Number of NDF events (pointer #1 in virtual concatenation)
- Corresponding clock deviation (pointer #1 in virtual concatenation)
- Differences (delta) between the pointer values of pointers #2 to #4 and pointer #1 (virtual concatenation)
- AU-NDF and NDF-P can be indicated by the LED display on the front panel (Application Manager - “Configuration” menu - LED Display ...):
  – the “AU-LOP/LOP-P” LED indicates “AU-NDF” in addition to “AU-LOP” and it indicates “NDF-P” in addition to “LOP-P”

Absolute pointer values, increments, decrements, sum of increments + decrements and NDF (pointer #1 in virtual concatenation) are displayed as histograms with a selectable time resolution of seconds, minutes, hours or days.

The differences (delta) between the pointer values of pointers #2 to #4 and pointer #1 are indicated as number of pointers and as time (µs) (virtual concatenation).

Printout

Absolute pointer values, increments, decrements, sum of increments + decrements, NDF and delta pointer (virtual concatenation) are printed out as a table with a resolution of 1 second.

2.3.4 Anomaly measurements

Evaluation

All anomalies are counted and recorded simultaneously.

Gate times . . . . . 1 to 99 seconds
or 1 to 99 minutes
or 1 to 99 hours
or 1 to 99 days

Intermediate results . . . . . 1 to 99 seconds
or 1 to 99 minutes

Display

Anomalies are indicated by LEDs:

CURRENT LED (red) is on while the anomaly is present.

HISTORY LED (yellow)is on if the anomaly occurred at least once or is still present during the current measurement interval.

Anomaly	LED
OOF-622	LOF/OOF
B1 (OC-12c/STM-4c)	B1/B2
B2 (OC-12c/STM-4c)	B1/B2
REI-L (OC-12c) MS-REI (STM-4c)	-
B3 (STS-12c SPE/VC-4-4c)	B3
REI-P (OC-12c) HP-REI (STM-4c)	-

Table S-10 LED display of anomalies

Evaluation and display of B2 errors refers to the concatenated data stream (BIP-96).

Evaluation and display of B3 errors:

- Contiguous concatenation: BIP-8
- Virtual concatenation: BIP-32

2.3.5 Defect detection

Evaluation

All defects that are present are evaluated and recorded simultaneously as far as possible. Recording takes place only within a started measurement interval.

Time resolution of defects . . . . . .100 ms

Display

Defects are indicated by LEDs:

CURRENT LED (red) is on while the defect is present.

HISTORY LED (yellow)is on if the defect occurred at least once or is still present during the current measurement interval.

Defect	LED
LOS (optical)	LOS
LOF-622	LOF/OOF
TIM-L (OC-12c) RS-TIM (STM-4c)	-
AIS-L (OC-12c) MS-AIS (STM-4c)	MS-AIS/AIS-L
RDI-L (OC-12c) MS-RDI (STM-4c)	MS-RDI/RDI-L
LOP-P (STS-12c SPE) AU-LOP (VC-4-4c)	AU-LOP/LOP-P
LOP-Cx[1]	AU-LOP/LOP-P
AIS-P (STS-12c SPE) AU-AIS (VC-4-4c)	AU-AIS/AIS-P
AIS-Cx[2]	AU-AIS/AIS-P AU-LOP/LOP-P
DPOVC[3]	AU-LOP/LOP-P
UNEQ-P (STS-12c SPE) HP-UNEQ (VC-4-4c)[4]	HP-UNEQ/UNEQ-P
PLM-P (STS-12c SPE) HP-PLM (VC-4-4c)	HP-PLM/PLM-P
RDI-P (STS-12c SPE) HP-RDI (VC-4-4c)	HP-RDI/RDI-P
TIM-P (STS-12c SPE) HP-TIM (VC-4-4c)	-

1 AU-LOP is indicated if LOP is detected in at least one AU-4 pointer.
2 AU-AIS is indicated if AIS is detected in all four AU-4 pointers.
If AU-AIS is detected in one, two or three AU-4 pointers, AU-LOP-LOP-P is indicated.
3 Virtual concatenation: DPOVC (**D**elta **P**ointer **O**verflow **V**irtual **C**oncatenation; Delta >± 40)
This defect is indicated if the maximum delta of one of the pointers #2 to #4 relative to pointer #1 is exceeded.
4 Virtual concatenation: HP-UNEQ/UNEQ-P is indicated if HP-UNEQ/UNEQ-P is detected in at least one of the four VC-4 containers.

Table S-11 LED display of defects

2.4 Payload

2.4.1 BULK signal receiver

Only with option BN 3035/90.90

2.4.1.1 Bit pattern payloads

See Sec. 1.4.1.1, Page S-10 and Sec. 1.4.1.2, Page S-10

2.4.1.2 Anomaly measurements

The following anomaly can be indicated and evaluated in addition to the anomalies described in Sec. 2.3.4, Page S-18:

Anomaly	LED
TSE	TSE

Table S-12 LED display of additional anomaly

2.4.1.3 Defect detection

The following defect can be indicated and evaluated in addition to the defects described in Sec. 2.3.5, Page S-19:

Defect	LED
LSS	LSS

Table S-13 LED display of additional defect

2.4.2 ATM receiver section

Only with options BN 3035/90.70 and BN 3035/90.91

2.4.2.1 Descrambling

Descrambling is according to ITU-T Recommendation I.432 ($X^{43}+1$).
The function can be disabled.

2.4.2.2 Measurement modes

2.4.2.3 Anomaly measurements

The following anomalies can be indicated and evaluated in addition to the anomalies described in Sec. 2.3.4, Page S-18.

Anomaly	LED	Explanation	
HCOR	-	Correctable Header Error	
HUNC	-	Uncorrectable Header Error	
CER	-	Cell Error Ratio	for measurements using test cells
CLR	-	Cell Loss Ratio	
CMR	-	Cell Misinsertion Rate	
AAL-1-CRC	-	AAL1 CRC Error	for AAL-1 measurements
AAL-1-PE	-	AAL1 Parity Error	
AAL-1-CLR	-	AAL1 Cell Loss Ratio	
AAL-1-CMR	-	AAL1 Cell Misinsertion Rate	

Table S-14 Indication and evaluation of anomalies

The anomalies HUNC and HCOR apply to the complete cell stream. All other anomalies apply to the measurement channel only.

2.4.2.4 Defect detection

The following defects can be indicated and evaluated in addition to the defects described in Sec. 2.3.5, Page S-19.

Defect	LED	Explanation	
LCD	LOF / LCD	Loss of Frame / Loss of Cell Delineation	
OCR	LOF / LCD	Overflow Cell Rate[1]	
OCLR	-	Cell Loss Overflow[2]	for measurements using test cells
OCMR	-	Cell Misinserted Overflow[3]	
VC-AIS	-	Virtual Channel Alarm Indication Signal	
VC-RDI	-	Virtual Channel Remote Defect Indication	
VP-AIS	-	Virtual Path Alarm Indication Signal	
VP-RDI	-	Virtual Path Remote Defect Indication	
AAL-1-OOS	-	AAL1 Out of Sync	

1 Test channel: Maximum cell rate (CBR) = 149760 kbit/s;
Max. consecutive cells at 599040 kbit/s = 400
2 More than 255 cell losses in 100 ms or relative to the last test cell
3 More than 255 misinserted cells in 100 ms or relative to the last test cell

Table S-15 LED display of additional defects

2.4.2.5 ATM performance measurements

Error-related performance parameters

The measurements are made using test cells.

Results

Lost Cell Count, Cell Loss Ratio . . . . . CLR
Misinserted Cell Count, Cell Misinserted Rate . . . . . CMR
Error Cell Count, Cell Error Ratio . . . . . CER

Cell transfer delay

The measurement is made using test cells.

Display . . . . . rate distribution
Resolution . . . . . 160 ns to 0.355 s
Measurement range . . . . . 20 µs to 42.9 s
Measurement range offset . . . . . 0 to 0.167 s
Units . . . . . µs

Cells with transfer delays outside the measurement range are counted as class 0 (underflow) or class 127 (overflow).

Cell delay variation

The measurement is made using test cells.

Display . . . . . rate distribution,
minimum delay,
maximum delay,
average delay,
peak-to-peak-CDV

The results are only valid if no cell delays outside the measurement range are detected.

2.4.3 User channel analysis and load measurement

Cell filters (VCI, VPI, CLP) for extracting the test channel.

The VCI and CLP filters can be disabled

Mean cell rate

The measurement is made over all connections in parallel and in the test channel simultaneously.

Measurement interval . . . . . 1 s
Resolution 0.01%

Load display

Units . . . . . Mbit/s, Cells/s, %
Scaling . . . . . linear, logarithmic

Peak cell rate

The measurement is made in the test channel.

Measurement interval . . . . . 1 s
Resolution 0.1%

Load display

Units . . . . . Mbit/s, Cells/s, %
Scaling . . . . . linear, logarithmic

Channel loading histogram

The channel loading histogram indicates the distribution of 100 ms measurement intervals according to measured load.

Measurement interval . . . . . 100 ms
Number of classes 101
Class “0” contains the number of 100 ms intervals in which a load of 0% was measured.
Class width 1%
Load display . . . . . Mbit/s, Cells/s, %

User channel cell distribution

Display of cells in the user channel classified as user cells, OAM cells and user cells with CLP indicator.

Measurement interval . . . . . 1 s
Display . . . . . cell count

Test channel

Maximum cell rate (CBR) . . . . . 149760 kbit/s

Max. consecutive cells at 599040 kbit/s . . . . . 400 cells

Test cell format

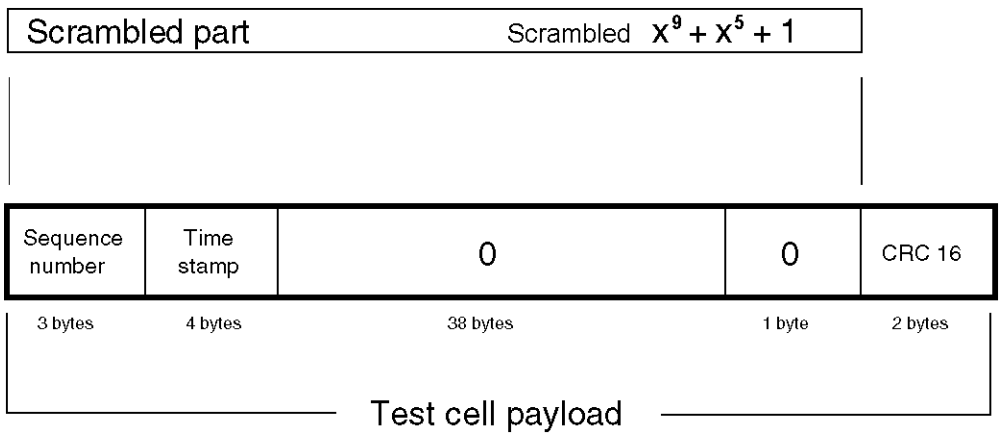


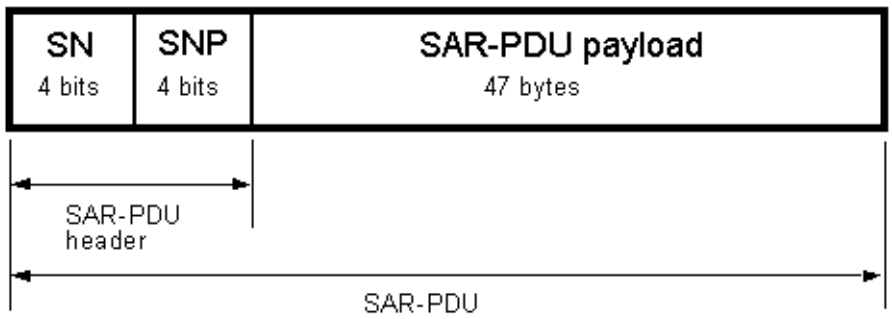
Fig. S-3 Test cell format to ITU-T O.191 (Draft 4/95)

2.4.3.1 AAL-1 reassembly

AAL-1 structured cells are reassembled from the SAR-PDU. The format is shown in the figure below. The TSE measurement is performed using framed or unframed pseudo-random bit sequences (PRBS) mapped into the SAR-PDU payload.

The following payload patterns are available for measurements:

- PRBS unframed
- PRBS in PCM-30 frame
- PRBS in PCM-30 frame (with CRC)



SN: Sequence Number
SNP: Sequence Number Protection
PDU: Protocol Data Unit
SAR: Segmentation and Reassembly

Fig. S-4 SAR-PDU format for AAL-1 cells

Notes:

Specifications OC-48c/STM-16c

These specifications apply to the following options:

OC-48c/STM-16c mappings

OC-12c/STM-4c ERROR TEST (BULK). . . . . .BN 3035/90.90
OC-12c/STM-4c ATM TESTING. . . . . .BN 3035/90.91
OC-48c/STM-16c ERROR TEST (BULK). . . . . .BN 3035/90.93

One of the following options is also required:

STM-16/OC-48 (1550 nm) . . . . . .BN 3035/91.53
STM-16/OC-48 (1310 nm) . . . . . .BN 3035/91.54
STM-16/OC-48 (1550 nm/1310 nm). . . . . .BN 3035/91.59

The numbers in square brackets [...] correspond to the numbers printed on the instrument.

Calibrated specifications are indicated by ***.

1 Generator section

1.1 Digital signal output

1.1.1 Signal output [47], optical

Connector . . . . . 2.5 mm (PC)

“Fiber-to-fiber” adapter for direct connection to various
2.5 mm connector types . . . . . see list of accessories

Output level *** . . . . . 0 dBm +0/-2 dBm

Output signal pulse shape . . . . . .to ITU-T G.957

Wavelength (switchable, depending on option) . . . . . 1310 nm (1285 to 1340 nm)
1550 nm (1520 to 1600 nm)

Laser class to EN 60825-1:1994
Normal operation 1
Fault condition 3A

The generator fulfils the requirements of ITU-T G.957, classes S16.2, L16.2, L16.3 or S16.1, L16.1.

LASER ON status display

LED is on when the laser source is active.

1.1.2 Signal output [46], electrical

Connector . . . . . unbalanced (coaxial)

Socket . . . . . SMA

Signal output impedance . . . . . 50 Ω

Line code . . . . . NRZ (scrambled)

Output voltage . . . . . ≥ 500 mVpp

Bit rate . . . . . 2488.32 Mbit/s

1.2 Clock generator and bit rates

1.2.1 Clock generation internal

See “Specifications” for the mainframe instrument.

Permissible clock offset . . . . . ± 50 ppm

1.2.2 Clock generation external [45]

For feeding in a jitter-modulated clock signal that must be derived from the base module clock.

Clock frequency . . . . . 2488.32 Mbit/s

Connector . . . . . unbalanced (coaxial)

Socket . . . . . SMA

Clock input impedance . . . . . 50 Ω

Input voltage range . . . . . .300 mVpp to 1 Vpp

1.2.3 Bit rate

STM-16, OC-48 . . . . . 2488.32 Mbit/s

1.3 SDH and SONET TX signals

- Generates an OC-48c signal conforming to the Bellcore-GR-253 standards.
- Generates an STM-16c signal conforming to ITU-T recommendation G.707.

1.3.1 OC-48c/STM-16c TX signals

OC-48c/STM-16c signal formation:

- Internally generated signal: The payload in 4 x STS-12c SPE/VC-4-4c contains a “Bulk” signal or ATM cells.
- Internally generated signal: The payload of one STS-12c SPE/VC-4-4c signal contains a “Bulk” signal or ATM cells. The other three STS-12c SPE/VC-4-4c signals are filled with HP-UNEQ
- Internally generated signal: The payload of the STS-48c SPE/VC-4-16c signals contains a “Bulk” signal
- Signal taken completely from receiver

1.3.2 Scrambling

Scrambling is as per ITU-T recommendation G.707.
The scrambler cannot be switched off.

1.3.3 Overhead generator

1.3.3.1 Section overhead (SOH), Transport overhead (TOH)

STM-16, OC-48 section overhead

see Sec. 16, Page S-31

Settings can be made in the entire SOH, TOH excluding the B1 and B2 bytes and the complete pointer line (H1, H2, H3).

XX: Inserted by parity formation (B1, B2)

Line 4a: SDH pointers (AU-4)

Line 4b: SDH pointers (AU-3)

Line 4c: SONET pointers (STS-1 SPE)

Line 4d: SONET pointers (STS-3c)

Line 4e: SDH pointers (AU-4, VC-4-4c)

Line 4f: SONET pointers (STS-12c SPE)

Line 4g: SDH pointers (AU-4, VC-4-16c)

Line 4h: SONET pointers (STS-48c SPE)

Line 9: Z1 and Z2 are used for SONET only

H1 and H2 depend on the pointer address setting (pointer address = 0 is shown). H3 depends on whether a pointer action takes place or not.

Overhead byte loading

- Static bytes: All except B1, B2, H1, H2, H3
- Overhead Sequence m, n, p: All except B1, B2, H1, H2, H3
- Trace Identifier: J0 (Length = 16 frames with CRC7 formation)
- Dynamic byte groups with pseudo random bit sequence PRBS11: E1, F1, E2
D1 to D3, D4 to D12 (byte group)
- Dynamic via DCC/ECC interface socket [40] (V.11): E1, F1, E2 (single byte)
- Dynamic via DCC/ECC interface socket [40] (V.11): D1 to D3, D4 to D12, K1 to K2 (byte group)

SOH, TOH	SOH	#1	#2	#3	#4	#5	#6	#7	#8	#9	#10	#11	#12	#13	#14	#15	#16	#1	...	#1	...	#16
	1	A1 A1 A1 F6 F6 F6	-- -- -- 00 00 00	-- -- -- 00 00 00	-- -- -- 00 00 00	-- -- -- 00 00 00	-- -- -- 00 00 00	-- -- -- 00 00 00	-- -- -- 00 00 00	-- -- -- 00 00 00	-- -- -- 00 00 00	-- -- -- 00 00 00	-- -- -- 00 00 00	-- -- -- 00 00 00	-- -- -- 00 00 00	-- -- -- 00 00 00	-- -- -- 00 00 00	J0 C1 10	-- -- -- 00 00 00	-- -- -- 00 00 00	-- -- -- 00 00 00	-- -- -- 00 00 00
	2	B1 XX	-- 00 00	-- 00 00	-- 00 00	-- 00 00	-- 00 00	-- 00 00	-- 00 00	-- 00 00	-- 00 00	-- 00 00	-- 00 00	-- 00 00	-- 00 00	-- 00 00	-- 00 00	J0 C1 0F	-- 00 00	-- 00 00	-- 00 00	-- 00 00
	3	D1 00	-- 00 00	-- 00 00	-- 00 00	-- 00 00	-- 00 00	-- 00 00	-- 00 00	-- 00 00	-- 00 00	-- 00 00	-- 00 00	-- 00 00	-- 00 00	-- 00 00	-- 00 00	J0 C1 0E	-- 00 00	-- 00 00	-- 00 00	-- 00 00
	4a	H1 68	H1 H1 H1 68 68 68	H1 H1 H1 68 68 68	H1 H1 H1 68 68 68	H1 H1 H1 68 68 68	H1 H1 H1 68 68 68	H1 H1 H1 68 68 68	H1 H1 H1 68 68 68	H1 H1 H1 68 68 68	H1 H1 H1 68 68 68	H1 H1 H1 68 68 68	H1 H1 H1 68 68 68	H1 H1 H1 68 68 68	H1 H1 H1 68 68 68	H1 H1 H1 68 68 68	H1 H1 H1 68 68 68	J0 C1 0D	H3 H3 H3 00 00 00	H3 H3 H3 00 00 00	H3 H3 H3 00 00 00	H3 H3 H3 00 00 00
	4b	H1 68	H1 H1 H1 68 68 68	H1 H1 H1 68 68 68	H1 H1 H1 68 68 68	H1 H1 H1 68 68 68	H1 H1 H1 68 68 68	H1 H1 H1 68 68 68	H1 H1 H1 68 68 68	H1 H1 H1 68 68 68	H1 H1 H1 68 68 68	H1 H1 H1 68 68 68	H1 H1 H1 68 68 68	H1 H1 H1 68 68 68	H1 H1 H1 68 68 68	H1 H1 H1 68 68 68	H1 H1 H1 68 68 68	J0 C1 0C	H3 H3 H3 00 00 00	H3 H3 H3 00 00 00	H3 H3 H3 00 00 00	H3 H3 H3 00 00 00
	4c	H1 60	H1 H1 H1 60 60 60	H1 H1 H1 60 60 60	H1 H1 H1 60 60 60	H1 H1 H1 60 60 60	H1 H1 H1 60 60 60	H1 H1 H1 60 60 60	H1 H1 H1 60 60 60	H1 H1 H1 60 60 60	H1 H1 H1 60 60 60	H1 H1 H1 60 60 60	H1 H1 H1 60 60 60	H1 H1 H1 60 60 60	H1 H1 H1 60 60 60	H1 H1 H1 60 60 60	H1 H1 H1 60 60 60	J0 C1 0B	H3 H3 H3 00 00 00	H3 H3 H3 00 00 00	H3 H3 H3 00 00 00	H3 H3 H3 00 00 00
	4d	H1 60	H1 H1 H1 60 60 60	H1 H1 H1 60 60 60	H1 H1 H1 60 60 60	H1 H1 H1 60 60 60	H1 H1 H1 60 60 60	H1 H1 H1 60 60 60	H1 H1 H1 60 60 60	H1 H1 H1 60 60 60	H1 H1 H1 60 60 60	H1 H1 H1 60 60 60	H1 H1 H1 60 60 60	H1 H1 H1 60 60 60	H1 H1 H1 60 60 60	H1 H1 H1 60 60 60	H1 H1 H1 60 60 60	J0 C1 0A	H3 H3 H3 00 00 00	H3 H3 H3 00 00 00	H3 H3 H3 00 00 00	H3 H3 H3 00 00 00
	4e	H1 68	Y Y Y 9B 9B 9B	Y Y Y 9B 9B 9B	Y Y Y 9B 9B 9B	Y Y Y 9B 9B 9B	Y Y Y 9B 9B 9B	Y Y Y 9B 9B 9B	Y Y Y 9B 9B 9B	H1 H1 H1 68 68 68	Y Y Y 9B 9B 9B	Y Y Y 9B 9B 9B	Y Y Y 9B 9B 9B	Y Y Y 9B 9B 9B	Y Y Y 9B 9B 9B	Y Y Y 9B 9B 9B	Y Y Y 9B 9B 9B	J0 C1 09	H3 H3 H3 00 00 00	H3 H3 H3 00 00 00	H3 H3 H3 00 00 00	H3 H3 H3 00 00 00
	4f	H1 60	Y Y Y 93 93 93	Y Y Y 93 93 93	Y Y Y 93 93 93	Y Y Y 93 93 93	Y Y Y 93 93 93	Y Y Y 93 93 93	H1 H1 H1 60 60 60	H1 H1 H1 60 60 60	Y Y Y 93 93 93	Y Y Y 93 93 93	Y Y Y 93 93 93	Y Y Y 93 93 93	Y Y Y 93 93 93	Y Y Y 93 93 93	Y Y Y 93 93 93	J0 C1 08	H3 H3 H3 00 00 00	H3 H3 H3 00 00 00	H3 H3 H3 00 00 00	H3 H3 H3 00 00 00
	4g	H1 68	Y Y Y 9B 9B 9B	Y Y Y 9B 9B 9B	Y Y Y 9B 9B 9B	Y Y Y 9B 9B 9B	Y Y Y 9B 9B 9B	Y Y Y 9B 9B 9B	Y Y Y 9B 9B 9B	Y Y Y 9B 9B 9B	H1 H1 H1 68 68 68	Y Y Y 9B 9B 9B	Y Y Y 9B 9B 9B	Y Y Y 9B 9B 9B	Y Y Y 9B 9B 9B	Y Y Y 9B 9B 9B	Y Y Y 9B 9B 9B	J0 C1 07	H3 H3 H3 00 00 00	H3 H3 H3 00 00 00	H3 H3 H3 00 00 00	H3 H3 H3 00 00 00
	4h	H1 60	Y Y Y 93 93 93	Y Y Y 93 93 93	Y Y Y 93 93 93	Y Y Y 93 93 93	Y Y Y 93 93 93	Y Y Y 93 93 93	Y Y Y 93 93 93	Y Y Y 93 93 93	Y Y Y 93 93 93	H1 H1 H1 60 60 60	Y Y Y 93 93 93	Y Y Y 93 93 93	Y Y Y 93 93 93	Y Y Y 93 93 93	Y Y Y 93 93 93	J0 C1 06	H3 H3 H3 00 00 00	H3 H3 H3 00 00 00	H3 H3 H3 00 00 00	H3 H3 H3 00 00 00
	5	B2 XX	B2 B2 B2 XX XX XX	B2 B2 B2 XX XX XX	B2 B2 B2 XX XX XX	B2 B2 B2 XX XX XX	B2 B2 B2 XX XX XX	B2 B2 B2 XX XX XX	B2 B2 B2 XX XX XX	B2 B2 B2 XX XX XX	B2 B2 B2 XX XX XX	B2 B2 B2 XX XX XX	B2 B2 B2 XX XX XX	B2 B2 B2 XX XX XX	B2 B2 B2 XX XX XX	B2 B2 B2 XX XX XX	B2 B2 B2 XX XX XX	K1 00	K2 00	-- -- -- 00 00 00	-- -- -- 00 00 00	-- -- -- 00 00 00
	6	D4 00	-- -- -- 00 00 00	-- -- -- 00 00 00	-- -- -- 00 00 00	-- -- -- 00 00 00	-- -- -- 00 00 00	-- -- -- 00 00 00	-- -- -- 00 00 00	-- -- -- 00 00 00	-- -- -- 00 00 00	-- -- -- 00 00 00	-- -- -- 00 00 00	-- -- -- 00 00 00	-- -- -- 00 00 00	-- -- -- 00 00 00	-- -- -- 00 00 00	D5 00	D6 00	-- -- -- 00 00 00	-- -- -- 00 00 00	-- -- -- 00 00 00
	7	D7 00	-- -- -- 00 00 00	-- -- -- 00 00 00	-- -- -- 00 00 00	-- -- -- 00 00 00	-- -- -- 00 00 00	-- -- -- 00 00 00	-- -- -- 00 00 00	-- -- -- 00 00 00	-- -- -- 00 00 00	-- -- -- 00 00 00	-- -- -- 00 00 00	-- -- -- 00 00 00	-- -- -- 00 00 00	-- -- -- 00 00 00	-- -- -- 00 00 00	D8 00	D9 00	-- -- -- 00 00 00	-- -- -- 00 00 00	-- -- -- 00 00 00
	8	D10 00	-- -- -- 00 00 00	-- -- -- 00 00 00	-- -- -- 00 00 00	-- -- -- 00 00 00	-- -- -- 00 00 00	-- -- -- 00 00 00	-- -- -- 00 00 00	-- -- -- 00 00 00	-- -- -- 00 00 00	-- -- -- 00 00 00	-- -- -- 00 00 00	-- -- -- 00 00 00	-- -- -- 00 00 00	-- -- -- 00 00 00	-- -- -- 00 00 00	D11 00	D12 00	-- -- -- 00 00 00	-- -- -- 00 00 00	-- -- -- 00 00 00
	9	S1 00	Z1 Z1 Z1 00 00 00	Z1 Z1 Z1 00 00 00	Z1 Z1 Z1 00 00 00	Z1 Z1 Z1 00 00 00	Z1 Z1 Z1 00 00 00	Z1 Z1 Z1 00 00 00	Z1 Z1 Z1 00 00 00	Z1 Z1 Z1 00 00 00	Z1 Z1 Z1 00 00 00	Z1 Z1 Z1 00 00 00	Z1 Z1 Z1 00 00 00	Z1 Z1 Z1 00 00 00	Z1 Z1 Z1 00 00 00	Z1 Z1 Z1 00 00 00	Z1 Z1 Z1 00 00 00	Z2	E2 00	Z2 Z2 Z2 00 00 00	Z2 Z2 Z2 00 00 00	Z2 Z2 Z2 00 00 00

Table S-16 SOH, TOH contents; STM-16, OC-48

1.3.4 Path overhead (POH), high-order

1.3.4.1 Contiguous concatenation

Standard overhead

POH byte	POH	"Fixed Stuff" Column #2 to #4 Container: STS-12c SPE/VC-4-4c Fixed stuffing (3 columns)	"Fixed Stuff" Column #2 to #16 Container: STS-48c SPE/VC-4-16c Fixed stuffing (15 columns)
J1 (ASCII)	"WG HP-TRACE"	"00"	"00"
B3 (hex)	Inserted by parity formation	"00"	"00"
C2 (hex)	"13" for ATM mapping "FE" for BULK (STM-4) "01" for BULK (OC-12)	"00"	"00"
G1 (hex)	"00"	"00"	"00"
F2 (hex)	"00"	"00"	"00"
H4 (hex)	"FF"	"00"	"00"
F3 (hex)	"00"	"00"	"00"
K3 (hex)	"00"	"00"	"00"
N1 (hex)	"00"	"00"	"00"

Table S-17 POH contents

Contents of VC-4c POH #1 bytes

- Static bytes: All except B3, H4
- Overhead sequence m, n, p: All except B3, H4
- Trace Identifier: J1 (length = 16 frames with CRC7 formation)
- Dynamic bytes filled with PRBS11: F2 (byte)
- Dynamic bytes via DCC/ECC interface (V.11): F2, K3, N1 (byte)
- H4 sequence, switchable, 4 / 48 bytes

1.3.5 Generation of pointer actions

1.3.5.1 Contiguous concatenation

Stimulation

AU-4 pointer sequences

See “STM-1 mapping” and “STS-1 mapping” specifications.

Pointer jumps

Pointer jump from pointer value A to pointer value B (including setting a new pointer).

Pointer jumps are executed using NDF.
Pointer range A + B:

AU-4 . . . . . 0 to 782

1.3.6 OC-48c/STM-16c anomaly insertion

Anomaly insertion . . . . . B1, B2, B3 parity errors
REI-L/MS-REI, REI-P/HP-REI

Trigger modes . . . . . Single
or Rate

A bit error rate is inserted when Rate is selected.

Anomaly	**Single**	**Rate[1]**	**Burst m, n (frame)**
B1 (OC-48c/STM-16c)	yes	2E-5 to 1E-10	m = 1 to 196000
B2 (OC-48c/STM-16c)	yes	2E-3 to 1E-10	m = 1 to 196000
REI-L (OC-48c) MS-REI (STM-16c)	yes	2E-3 to 1E-10	m = 1 to 196000
B3 (STS-12c SPE/VC-4-4c)	yes	2E-4 to 1E-10	m = 1 to 196000
B3 (STS-48c SPE/VC-4-16c)	yes	2E-5 to 1E-10	m = 1 to 196000
REI-P (STS-12c SPE) HP-REI (VC-4-4c)	yes	2E-4 to 1E-10	m = 1 to 196000
REI-P (STS-48c SPE) HP-REI (VC-4-16c)	yes	2E-5 to 1E-10	m = 1 to 196000

1 Mantissa: 1 to 9, Exponent: -3 to -10 (integer values)

Table S-18 Anomalies (OC-12c/STM-16c) and trigger modes

Insertion of **anomalies** and **defects** is mutually exclusive. The action first selected is active; the second action is rejected.

1.3.7 OC-48c/STM-16c defect generation

Defect	**Sensor function test**	**Sensor threshold test**	
-	On / Off	M in N	|---t1---| |------t2------|
LOS (optical)	yes	M = 800 to 7200 N = 1600 to 8000	t1 = 0.1 to 60.0 s t2 = 0.2 to 600 s
LOF-2488	yes	M = 1 to N - 1 N = 1 to 8000	t1 = 0.1 to 60.0 s t2 = 0.2 to 600 s
TIM-L (OC-48c) RS-TIM (STM-16c)	yes	-	-
AIS-L (OC-48c) MS-AIS (STM-16c)	yes	M = 1 to N - 1 N = 1 to 8000	t1 = 0.1 to 60.0 s t2 = 0.2 to 600 s
RDI-L (OC-48c) MS-RDI (STM-16c)	yes	M = 1 to N - 1 N = 1 to 8000	t1 = 0.1 to 60.0 s t2 = 0.2 to 600 s
LOP_P (STS-12c SPE/STS-48c SPE)[1] AU-LOP (VC-4-4c/VC-4-16c)	yes	M = 1 to N - 1 N = 1 to 8000	t1 = 0.1 to 60.0 s t2 = 0.2 to 600 s
LOP-Cx[2]	yes	M = 1 to N - 1 N = 1 to 8000	t1 = 0.1 to 60.0 s t2 = 0.2 to 600 s
AIS-P (STS-12c SPE/STS-48c SPE)[1] AU-AIS (VC-4-4c/VC-4-16c)	yes	M = 1 to N - 1 N = 1 to 8000	t1 = 0.1 to 60.0 s t2 = 0.2 to 600 s
AIS-Cx[2]	yes	M = 1 to N - 1 N = 1 to 8000	t1 = 0.1 to 60.0 s t2 = 0.2 to 600 s
UNEQ-P (STS-12c SPE/STS-48c SPE) HP-UNEQ (VC-4-4c/VC-4-16c)	ja	M = 1 to N - 1 N = 1 to 8000	t1 = 0.1 to 60.0 s t2 = 0.2 to 600 s
PLM-P (STS-12c SPE/STS-48c SPE) HP-PLM (VC-4-4c/VC-4-16c)	yes	M = 1 to N - 1 N = 1 to 8000	t1 = 0.1 to 60.0 s t2 = 0.2 to 600 s
RDI-P (STS-12c SPE/STS-48c SPE) HP-RDI (VC-4-4c/VC-4-16c)	yes	M = 1 to N - 1 N = 1 to 8000	t1 = 0.1 to 60.0 s t2 = 0.2 to 600 s
TIM-P (STS-12c SPE/STS-48c SPE) HP-TIM (VC-4-4c/VC-4-16c)	yes	-	-

1 Insertion in all four pointers (AU-4) for STS-12c SPE/VC-4-4c
Insertion in all sixteen pointers (AU-4) for STS-48c SPE/VC-4-16c
2 X = 1 to 4 for STS-12c SPE/VC-4-4c
X = 1 to 16 for STS-48c SPE/VC-4-16c
Insertion in selected pointer (AU-4) only

Table S-19 Defects (OC-48c/STM-16c)

Insertion of **defects** and **anomalies** is mutually exclusive. The action first selected is active; the second action is rejected.

1.4 Payload generation

1.4.1 BULK signal generator

Only with option BN 3035/90.90 or BN 3035/90.93

1.4.1.1 Payload

Bit rate (STS-48c SPE/VC-4-16c) . . . . . 2396.16 Mbit/s
Bit rate (STS-12c SPE/VC-4-4c) . . . . . 599.04 Mbit/s

Structure . . . . . unframed

1.4.1.2 Bit patterns

Digital word . . . . . 16 bits

Pseudo-random bit sequences . . . . PRBS 23, PRBS 23 inverted, PRBS 31, PRBS 31 inverted

1.4.1.3 Anomaly insertion

The following anomaly can be inserted in addition to those described in Sec. 1.3.6, Page S-33:

Anomaly	**Single**	**Rate[1]**
TSE	yes	1E-3 to 1E-9
1 Mantissa: 1, Exponent -3 to -9 (integer values)		

Table S-20 Additional anomaly (STS-12c SPE/VC-4-4c, STS-48c/VC-4-16c)

Anomaly insertion . . . . . Test sequence error (TSE)

Trigger modes . . . . . Single or Rate

Insertion of **anomalies** and **defects** is mutually exclusive. The action first selected is active; the second action is rejected.

1.4.2 ATM generator for STS-12c SPE/VC-4-4c container

Only with options BN 3035/90.70 (ATM Module) and BN 3035/90.91

1.4.2.1 Scrambling

Scrambling is according to ITU-T Recommendation I.432 ($X^{43}+1$). The function can be disabled.

1.4.2.2 Anomaly insertion

The following anomalies can be inserted in addition to those described in Sec. 1.3.6, Page S-33.

Anomaly	**Single**	**Rate[1]**	**Sensor threshold**
			M in N
HEC uncor.[2]	yes	1E-2 to 1E-6	M = 1 to 31 N = M + 1 to M + 31
HEC cor.[3]	yes	1E-2 to 1E-6	M = 1 to 31 N = M + 1 to M + 31
AAL-1 cell loss	yes	1E-3 to 1E-6	-
AAL-1 CRC	yes	1E-3 to 1E-6	-
AAL-1 PE	yes	1E-3 to 1E-6	-

1 Mantissa: 1 only, Exponent: -1 to -6 (integer values)
2 Uncorrectable header error
3 Correctable header error

Table S-21 Additional anomalies

The AAL-1 cell loss, AAL-1 CRC and AAL-1 PE anomalies refer to the measurement channel. Test sequence errors (TSE) are inserted in the ATM payload or in the AAL-1 payload of the test channel.

Correctable and uncorrectable header errors are inserted in the overall cell stream.

1.4.2.3 Defect generation

The following defects can be generated in addition to those described in Sec. 1.3.7, Page S-34.

Defect	Sensor function test	Single
	On / Off	
LCD[1]	yes	yes
VP-AIS	yes	yes
VP-RDI	yes	yes
VC-AIS[2]	yes	yes
VC-RDI[3]	yes	yes
Vx-AIS[4]	yes	yes
Vx-RDI[4]	yes	yes

1 LCD (Loss of Cell Delineation) is generated by uncorrectable header errors in ≥ 7 consecutive cells.
2 AIS: Alarm Indication Signal; VC: Virtual Channel; VP: Virtual Path
3 RDI: Remote Defect Indication
4 For Vx-AIS and Vx-RDI defects are inserted in the VP and VC in parallel.

Table S-22 Additional defects

1.4.2.4 Test channel

Cells

Header

UNI/NNI, VCI, VPI, PT and CLP . . . . . settable
HEC . . . . . formed automatically

Payload

Pseudo-random bit sequences . . . . . PRBS 11, PRBS 15, PRBS 20, PRBS 23
Digital word . . . . . 16 bits

Load profiles

Constant, Equidistant, Burst

Constant load profile

Load setting . . . . . 14.976 to 149760 kbit/s

Resolution dependent on load range setting
14.976 to 1482.624 kbit/s . . . . . 14.976 kbit/s
149.76 to 14826.24 kbit/s . . . . . 149.76 kbit/s
1497.6 to 149760 kbit/s . . . . . 1497.6 kbit/s

Equidistant load profile setting range

Cell spacing . . . . . 4 to 40000 cell periods
Maximum cell spacing deviation . . . . . ± 1 cell period

Resolution depending on cell spacing range setting
4 to 400 . . . . . 4 cell periods
40 to 4000 . . . . . 40 cell periods
400 to 40000 . . . . . 400 cell periods

Burst load profile setting range

Maximum burst length . . . . . 4092 cells / 2.79 ms
Burst load . . . . . 1497.6 to 149760 kbit/s
Resolution . . . . . depends on burst length

Maximum burst period . . . . . 131068 cells / 89 ms

Load units . . . . . Mbit/s, Cells/s, %
Time units . . . . . cell period

1.4.2.5 Background load

A channel is generated as background load. The test channel has priority.

Header . . . . . freely selectable

Payload . . . . . byte by byte constant, bytes freely selectable

Load profile . . . . . CBR, Fill

Constant bit rate (CBR) . . . . . 449280 kbit/s

Filling up to . . . . . 149760 / 599040 kbit/s

1.4.2.6 Fill cells

The cell stream is filled with IDLE or UNASSIGNED cells. Either can be selected.

1.4.2.7 AAL-1 segmentation

PDU signals with system bandwidths of 1,5 Mbit/s, 2 Mbit/s, etc. can be transmitted in the AAL-1 in the test channel.

Possible payload patterns for 2 Mbit/s . . . . . PRBS unframed,
PRBS in PCM30,
PRBS in PCM30CRC

2 Receiver section

2.1 Digital signal inputs

2.1.1 Signal input [44], optical

Caution

Destruction of input [44]

The maximum input level of -8 dBm must not be exceeded. Otherwise, the optical input can be destroyed.

⇒ Insert an optical attenuator in any case:
- for RX - TX loop operation
- for higher input levels

Connector . . . . . 2.5 mm (PC)

“Fiber-to-fiber” adapter for direct connection to various
2.5 mm connector types . . . . . see list of accessories

Input sensitivity
STM-16/OC-48 *** . . . . . -8 to -28 dBm

Max. permitted input level . . . . . -8 dBm

Wavelength . . . . . 1100 to 1600 nm

The receiver meets the requirements of ITU-T G.957 classes S16.2, L16.2, L16.3 or S16.1 and L16.1.

Optical signal level display

Resolution . . . . . 1 dBm

Accuracy . . . . . ±3 dB

LOS (Loss of Signal) status display

LED is on when the signal input is active but no signal is present.

LOS threshold . . . . . < -30 dBm

2.1.2 Signal input [43], electrical

Connector . . . . . unbalanced (coaxial)

Type. . . . . SMA

Input impedance . . . . . 50 Ω

Line code . . . . . NRZ (scrambled)

Input voltage range . . . . . 300 mVpp to 1Vpp

Bit rate . . . . . 2488.32 Mbit/s

LOS (Loss of Signal) status display

LED is on when the signal input is active but no signal is present.

2.1.3 Clock output [42]

For the recovered receive clock

Frequency . . . . . 2488.32 MHz

Connector . . . . . unbalanced (coaxial)

Socket . . . . . SMA

Output impedance . . . . . 50 Ω

Output voltage . . . . . ≥ 100 mVpp

2.1.4 Clock recovery

See “Specifications” of the mainframe instrument.

2.2 SDH and SONET RX signals

- Evaluation of OC-48c signal conforming to Bellcore GR-253 standards.
- Evaluation of STM-16c signal conforming to ITU-T recommendation G.707.

2.2.1 OC-48c/STM-16c RX signal

OC-48c/STM-16c signal evaluation:

- Analysis of Transport Overhead (TOH) / Section Overhead (SOH), Path Overhead (POH) and payload (BULK) for STS-12c SPE/VC-4-4c containers either directly or in conjunction with the ATM module (option BN 3035/90.70).
- Analysis of Transport Overhead (TOH) / Section Overhead (SOH), Path Overhead (POH) and payload (BULK) for STS-48c SPE/VC-4-16c containers.
- Analysis of Transport Overhead (TOH) / Section Overhead (SOH) and loop-through of STS-12c SPE/VC-4-4c signal to transmitter (“Through” mode).

2.2.2 Descrambling

Descrambling is as per ITU-T recommendation G.707.
The descrambler cannot be switched off.

Tip: Make sure that there are no long sequences of zeros or ones in the data stream of unscrambled input signals.

2.3 Measurement modes

2.3.1 Evaluation of section overhead (SOH), transport overhead (TOH)

Display

Complete SOH, TOH: (16 channel-associated part SOH) . . . . . hexadecimal

Trace Identifier J0. . . . . .ASCII, plain text

Overhead Capture . . . . . .see Section 1 “Extended Overhead Analysis” option BN 3035/90.15

Evaluation

Bit error rate test

using pseudo-random bit sequence PRBS11 . . . . . E1, F1, E2 (single byte)

using pseudo-random bit sequence PRBS11 . . . . . .D1 to D3, D4 to D12 (byte group)

Output

The overhead channels are output via the

DCC/ECC interface, socket [21] (V.11) . . . . . E1, F1, E2 (single byte)

DCC/ECC interface, socket [21] (V.11) . . . . . D1 to D3, D4 to D12, K1 to K2 (byte group)

2.3.2 Evaluation of path overhead (POH)

2.3.2.1 Contiguous concatenation

Display

Complete POH . . . . . hexadecimal

Trace Identifier J1 . . . . . ASCII, plain text

Evaluation

Bit error rate test

using pseudo-random bit sequence PRBS11 . . . . . F2

Output

The overhead channels are output via the

DCC/ECC interface, socket [21] (V.11) F2, N1

2.3.3 Measurement of AU pointer actions

Evaluation

The AU pointer is indicated as an absolute value. The direction and number of pointer movements are detected.

NDF (new data flag) is detected and counted.

Display

- Number of AU pointer operations:
  Increments, decrements, sum of increments + decrements,
  difference of increments - decrements
- Pointer address
- Number of NDF events
- Corresponding clock deviation
- AU-NDF and NDF-P can be indicated by the LED display on the front panel
  (Application Manager - “Configuration” menu - LED Display ...):
  – the “AU-LOP/LOP-P” LED indicates “AU-NDF” in addition to “AU-LOP” and it indicates “NDF-P” in addition to “LOP-P”

Absolute pointer values, increments, decrements, sum of increments + decrements and NDF are displayed as histograms with a selectable time resolution of seconds, minutes, hours or days.

Printout

Absolute pointer values, increments, decrements, sum of increments + decrements and NDF are printed out as a table with a resolution of 1 second.

2.3.4 Anomaly measurements

Evaluation

All anomalies are counted and recorded simultaneously.

Gate times . . . . . 1 to 99 seconds
or 1 to 99 minutes
or 1 to 99 hours
or 1 to 99 days

Intermediate results . . . . . 1 to 99 seconds
or 1 to 99 minutes

Display

Anomalies are indicated by LEDs:

CURRENT LED (red) is on while the anomaly is present.

HISTORY LED (yellow)is on if the anomaly occurred at least once or is still present during the current measurement interval.

Anomaly	**LED**
OOF-2488	LOF/OOF
B1 (OC-48c/STM-16c)	B1/B2
B2 (OC-48c/STM-16c)	B1/B2
REI-L (OC-48c) MS-REI (STM-16c)	-
B3 (STS-12c SPE/STS-48c SPE/VC-4-4c/VC-4-16c)	B3
REI-P (STS-12c SPE/STS-48c SPE) HP-REI (VC-4-4c/VC-4-16c)	-

Table S-23 LED display of anomalies (OC-48c/STM-16c)

Evaluation and display of B2 errors refers to the concatenated data stream (BIP-384).

Evaluation and display of B3 errors for contiguous concatenation: BIP-8

2.3.5 Defect detection

Evaluation

All defects that are present are evaluated and recorded simultaneously as far as possible. Recording takes place only within a started measurement interval.

Time resolution of defects . . . . . .100 ms

Display

Defects are indicated by LEDs:

CURRENT LED (red) is on while the defect is present.

HISTORY LED (yellow)is on if the defect occurred at least once or is still present during the current measurement interval.

Defect	**LED**
LOS (optisch)	LOS
LOF-2488	LOF/OOF
TIM-L (OC-48c) RS-TIM (STM-16c)	-
AIS-L (OC-48c) MS-AIS (STM-16c)	MS-AIS/AIS-L
RDI-L (OC-48c) MS-RDI (STM-16c)	MS-RDI/RDI-L
LOP-P (STS-12c SPE/STS-48c SPE) AU-LOP (VC-4-4c/VC-4-16c)	AU-LOP/LOP-P
LOP-Cx[1]	AU-LOP/LOP-P
AIS-P (STS-12c SPE/STS-48c SPE)[1] AU-AIS (VC-4-4c/VC-4-16c)	AU-AIS/AIS-P
AIS-Cx[2]	AU-AIS/AIS-P AU-LOP/LOP-P
UNEQ-P (STS-12c SPE/STS-48c SPE) HP-UNEQ (VC-4-4c/VC-4-16c)	HP-UNEQ/UNEQ-P
PLM-P (STS-12c SPE/STS-48c SPE) HP-PLM (VC-4-4c/VC-4-16c)	HP-PLM/PLM-P
RDI-P (STS-12c SPE/STS-48c SPE) HP-RDI (VC-4-4c/VC-4-16c)	HP-RDI/RDI-P
TIM-P (STS-12c SPE/STS-48c SPE) HP-TIM (VC-4-4c/VC-4-16c)	-

1 AU-LOP is indicated if LOP is detected in at least one AU-4 pointer.
2 AU-AIS is indicated if AIS is detected in all four AU-4 pointers.
If AU-AIS is detected in one, two or three AU-4 pointers, AU-LOP-LOP-P is indicated.

Table S-24 LED display of defects (OC-48c/STM-16c)

2.4 Payload

2.4.1 BULK signal receiver

Only with option BN 3035/90.90 or BN 3035/90.93

2.4.1.1 Bit pattern payloads

See Sec. 1.4.1.1, Page S-35 and Sec. 1.4.1.2, Page S-35

2.4.1.2 Anomaly measurements

The following anomaly can be indicated and evaluated in addition to the anomalies described in Sec. 2.3.4, Page S-44:

Anomaly	LED
TSE	TSE

Table S-25 LED display of additional anomaly

2.4.1.3 Defect detection

The following defect can be indicated and evaluated in addition to the defects described in Sec. 2.3.5, Page S-45:

Defect	LED
LSS	LSS

Table S-26 LED display of additional defect

2.4.2 ATM receiver section

Only with option BN 3035/90.70 and BN 3035/09.91

2.4.2.1 Descrambling

Descrambling is according to ITU-T Recommendation I.432 ($X^{43}+1$).
The function can be disabled.

2.4.2.2 Measurement modes

2.4.2.3 Anomaly measurements

The following anomalies can be indicated and evaluated in addition to the anomalies described in Sec. 2.3.4, Page S-44.

Anomaly	LED	Explanation	
HCOR	-	Correctable Header Error	
HUNC	-	Uncorrectable Header Error	
CER	-	Cell Error Ratio	for measurements using test cells
CLR	-	Cell Loss Ratio	
CMR	-	Cell Misinsertion Rate	
AAL-1-CRC	-	AAL1 CRC Error	for AAL-1 measurements
AAL-1-PE	-	AAL1 Parity Error	
AAL-1-CLR	-	AAL1 Cell Loss Ratio	
AAL-1-CMR	-	AAL1 Cell Misinsertion Rate	

Table S-27 Indication and evaluation of anomalies

The anomalies HUNC and HCOR apply to the complete cell stream. All other anomalies apply to the measurement channel only.

2.4.2.4 Defect detection

The following defects can be indicated and evaluated in addition to the defects described in Sec. 2.3.5, Page S-45.

Defect	LED	Explanation	
LCD	LOF / LCD	Loss of Frame / Loss of Cell Delineation	
OCR	LOF / LCD	Overflow Cell Rate[1]	
OCLR	-	Cell Loss Overflow[2]	for measurements using test cells
OCMR	-	Cell Misinserted Overflow[3]	
VC-AIS	-	Virtual Channel Alarm Indication Signal	
VC-RDI	-	Virtual Channel Remote Defect Indication	
VP-AIS	-	Virtual Path Alarm Indication Signal	
VP-RDI	-	Virtual Path Remote Defect Indication	
AAL-1-OOS	-	AAL1 Out of Sync	

1 Test channel: Maximum cell rate (CBR) = 149760 kbit/s;
Max. consecutive cells at 599040 kbit/s = 400
2 More than 255 cell losses in 100 ms or relative to the last test cell
3 More than 255 misinserted cells in 100 ms or relative to the last test cell

Table S-28 LED display of additional defects

2.4.2.5 ATM performance measurements

Error-related performance parameters

The measurements are made using test cells.

Results

Lost Cell Count, Cell Loss Ratio . . . . . CLR
Misinserted Cell Count, Cell Misinserted Rate . . . . . CMR
Error Cell Count, Cell Error Ratio . . . . . CER

Cell transfer delay

The measurement is made using test cells.

Display . . . . . rate distribution
Resolution . . . . . 160 ns to 0.355 s
Measurement range . . . . . 20 µs to 42.9 s
Measurement range offset . . . . . 0 to 0.167 s
Units . . . . . µs

Cells with transfer delays outside the measurement range are counted as class 0 (underflow) or class 127 (overflow).

Cell delay variation

The measurement is made using test cells.

Display . . . . . rate distribution,
minimum delay,
maximum delay,
average delay,
peak-to-peak-CDV

The results are only valid if no cell delays outside the measurement range are detected.

2.4.3 User channel analysis and load measurement

Cell filters (VCI, VPI, CLP) for extracting the test channel.

The VCI and CLP filters can be disabled

Mean cell rate

The measurement is made over all connections in parallel and in the test channel simultaneously.

Measurement interval . . . . . 1 s
Resolution 0.01%

Load display

Units . . . . . Mbit/s, Cells/s, %
Scaling . . . . . linear, logarithmic

Peak cell rate

The measurement is made in the test channel.

Measurement interval . . . . . 1 s
Resolution 0.1%

Load display

Units . . . . . Mbit/s, Cells/s, %
Scaling . . . . . linear, logarithmic

Channel loading histogram

The channel loading histogram indicates the distribution of 100 ms measurement intervals according to measured load.

Measurement interval . . . . . 100 ms
Number of classes 101
Class “0” contains the number of 100 ms intervals in which a load of 0% was measured.
Class width 1%
Load display . . . . . Mbit/s, Cells/s, %

User channel cell distribution

Display of cells in the user channel classified as user cells, OAM cells and user cells with CLP indicator.

Measurement interval . . . . . 1 s
Display . . . . . cell count

Test channel

Maximum cell rate (CBR) . . . . . 149760 kbit/s

Max. consecutive cells at 599040 kbit/s . . . . . 400 cells

Test cell format

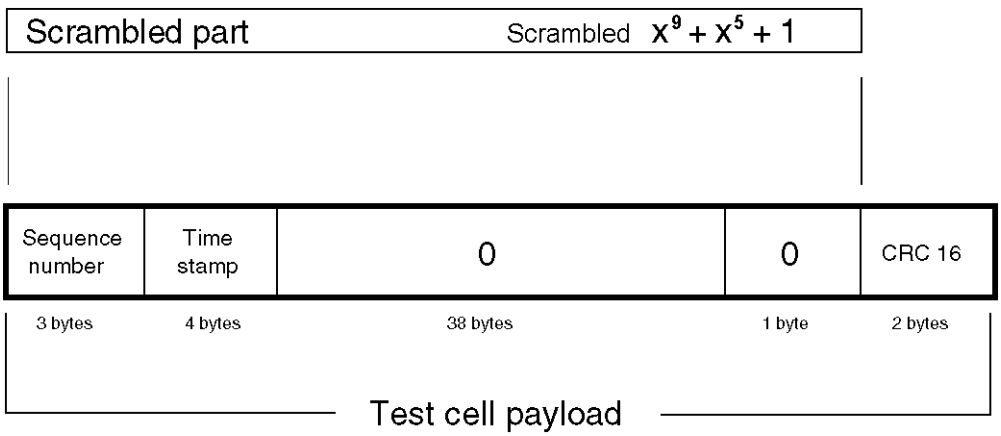


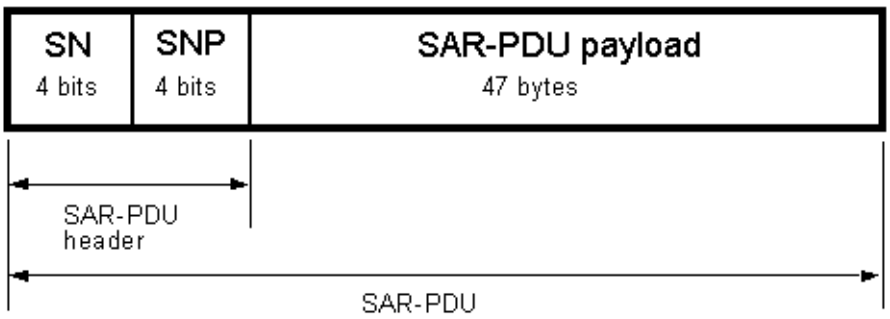
Fig. S-5 Test cell format to ITU-T O.191 (Draft 4/95)

2.4.3.1 AAL-1 reassembly

AAL-1 structured cells are reassembled from the SAR-PDU. The format is shown in the figure below. The TSE measurement is performed using framed or unframed pseudo-random bit sequences (PRBS) mapped into the SAR-PDU payload.

The following payload patterns are available for measurements:

- PRBS unframed
- PRBS in PCM-30 frame
- PRBS in PCM-30 frame (with CRC)



SN: Sequence Number
SNP: Sequence Number Protection
PDU: Protocol Data Unit
SAR: Segmentation and Reassembly

Fig. S-6 SAR-PDU format for AAL-1 cells